

Compal Confidential

FPI50 MB Schematic Document

LA-H329P

Version: 1.0

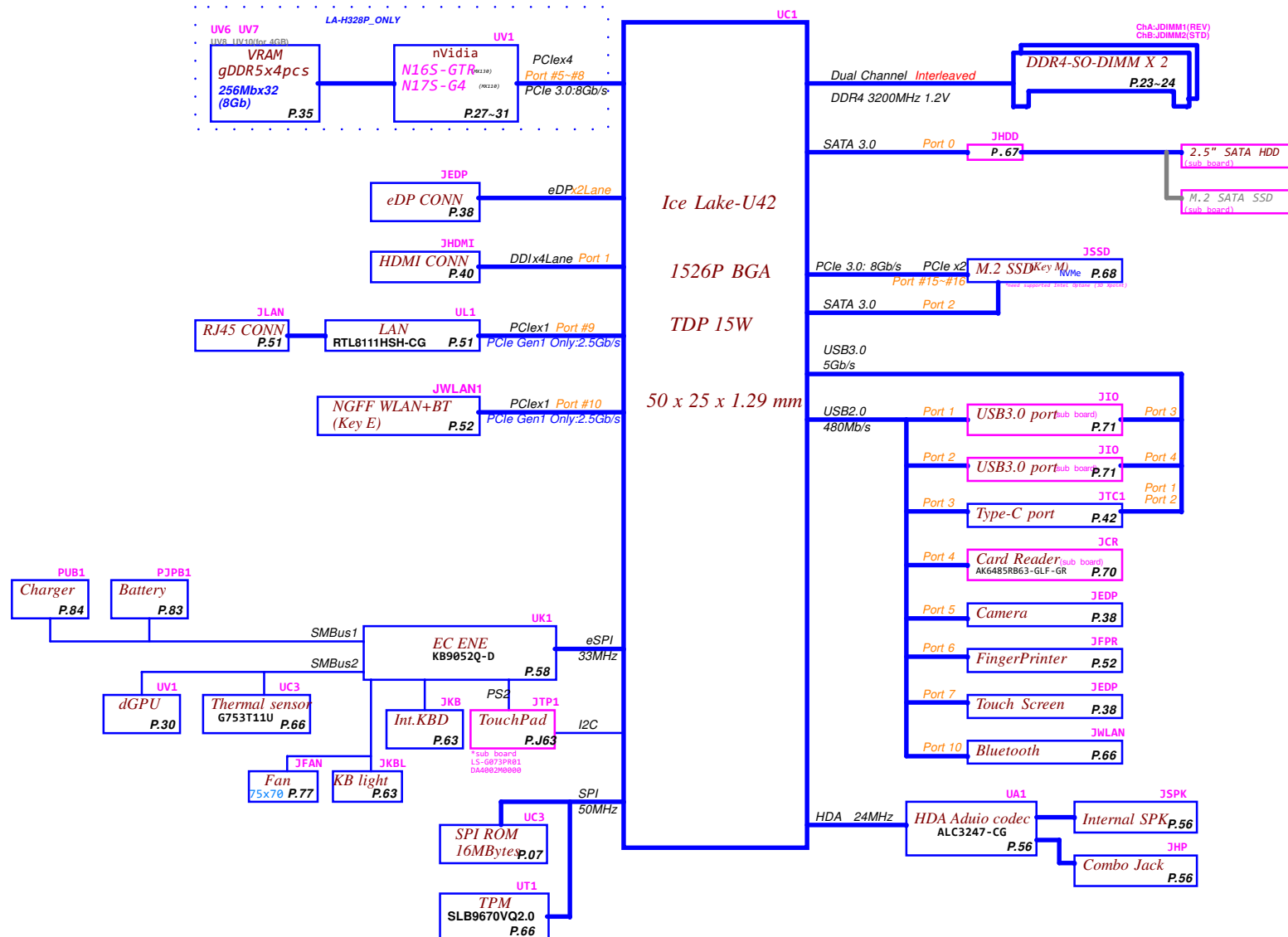
Date : 2020/01/15

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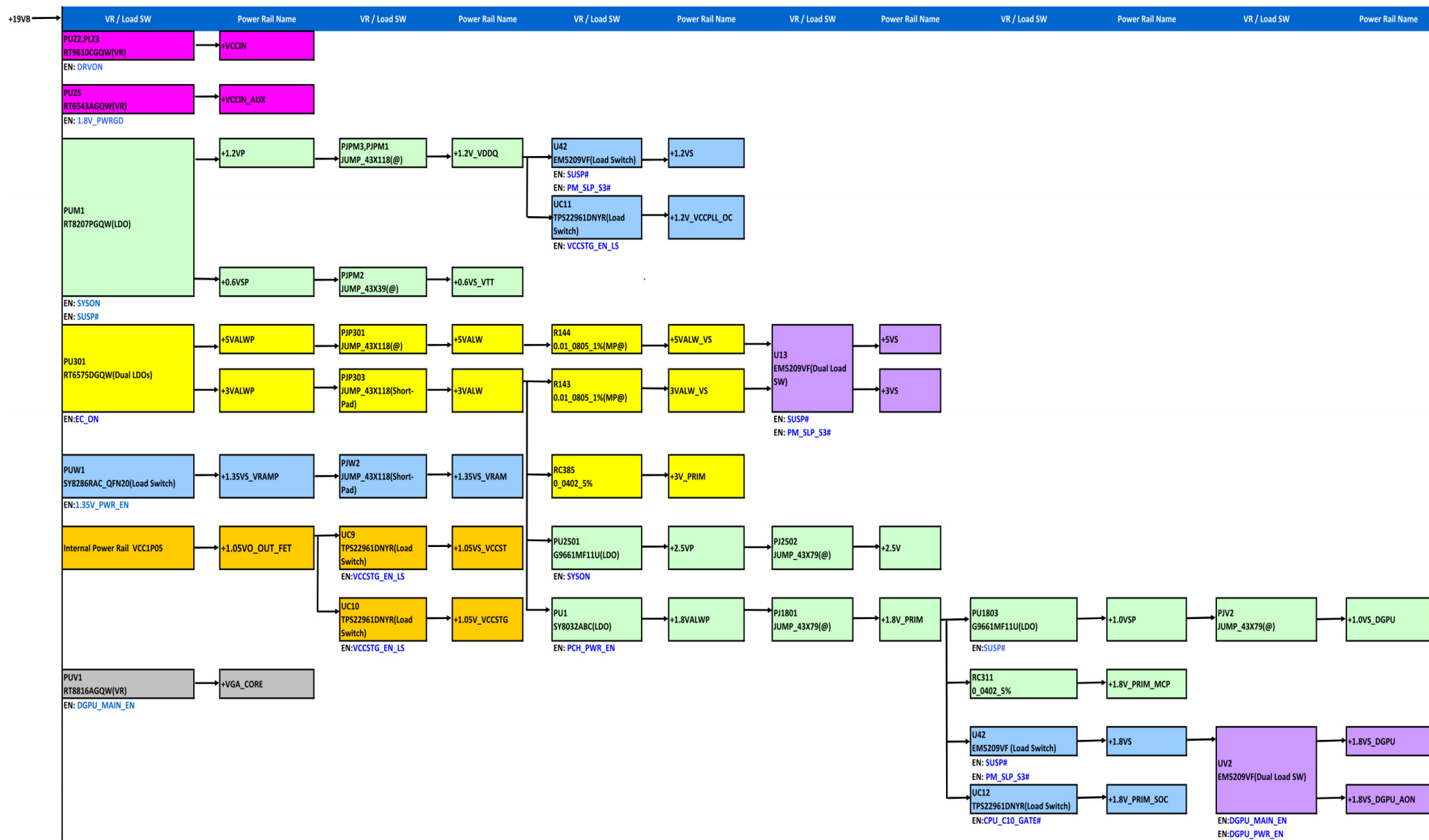
Model Name: ICL-U

Project Name: LA-H329P



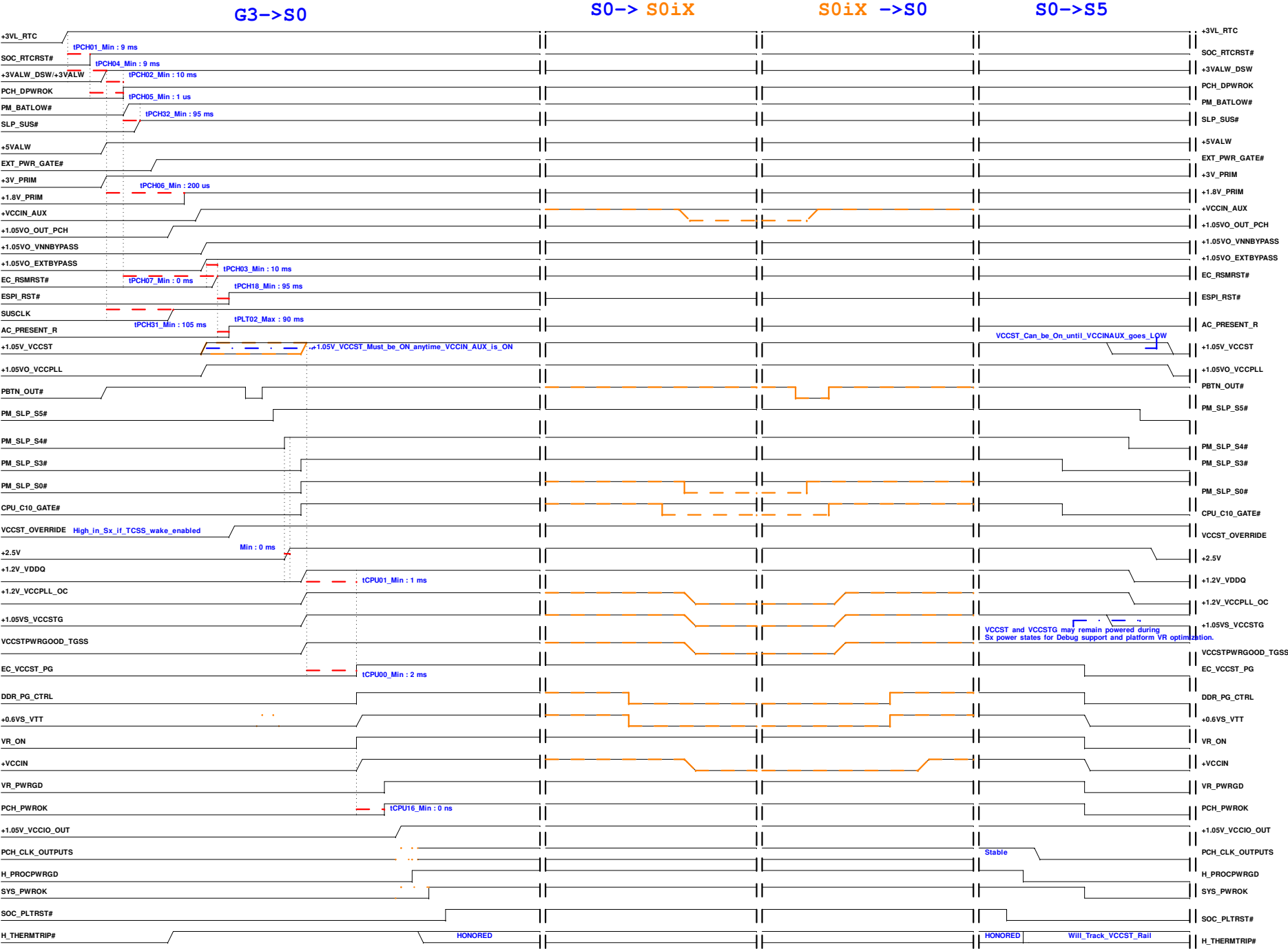
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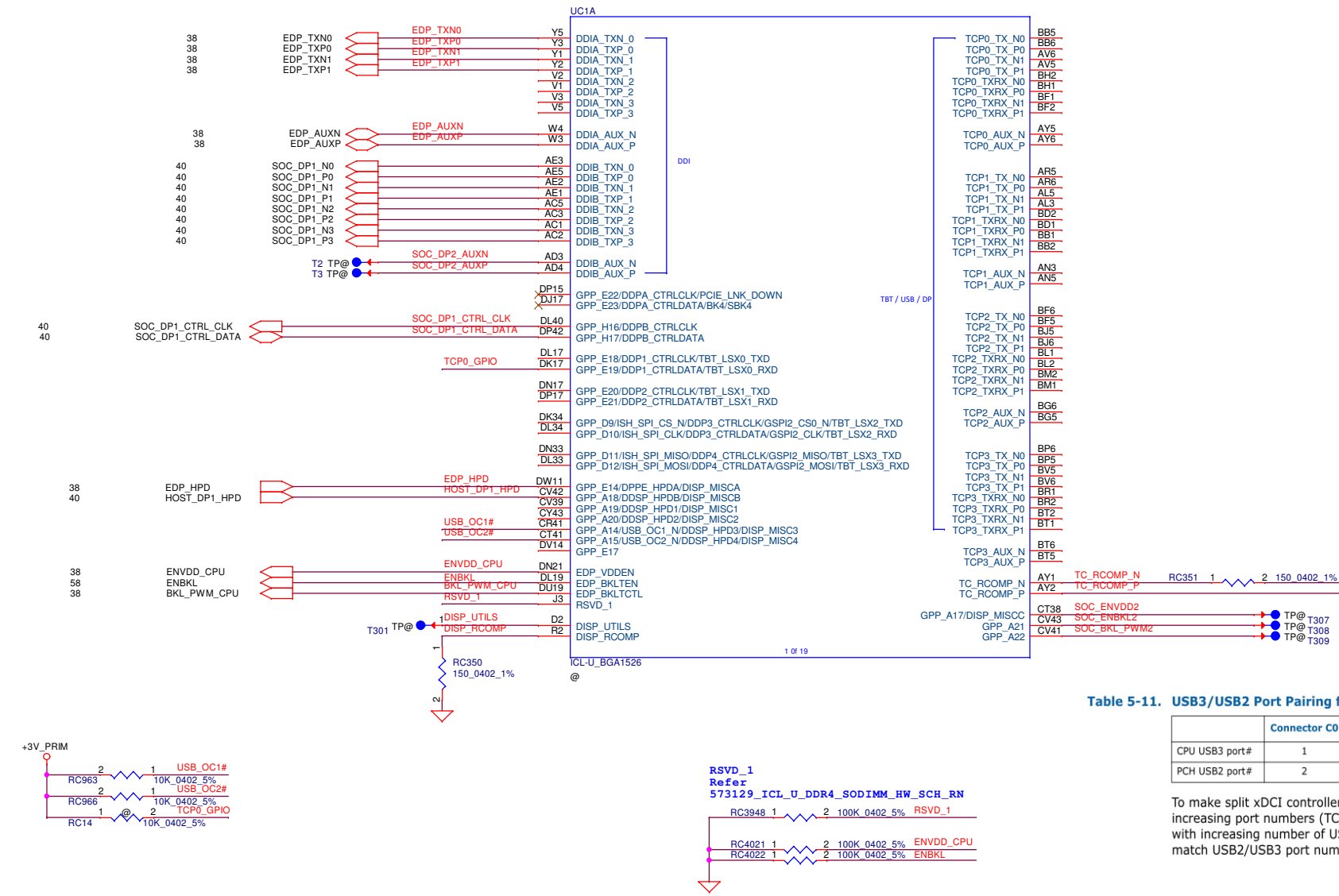
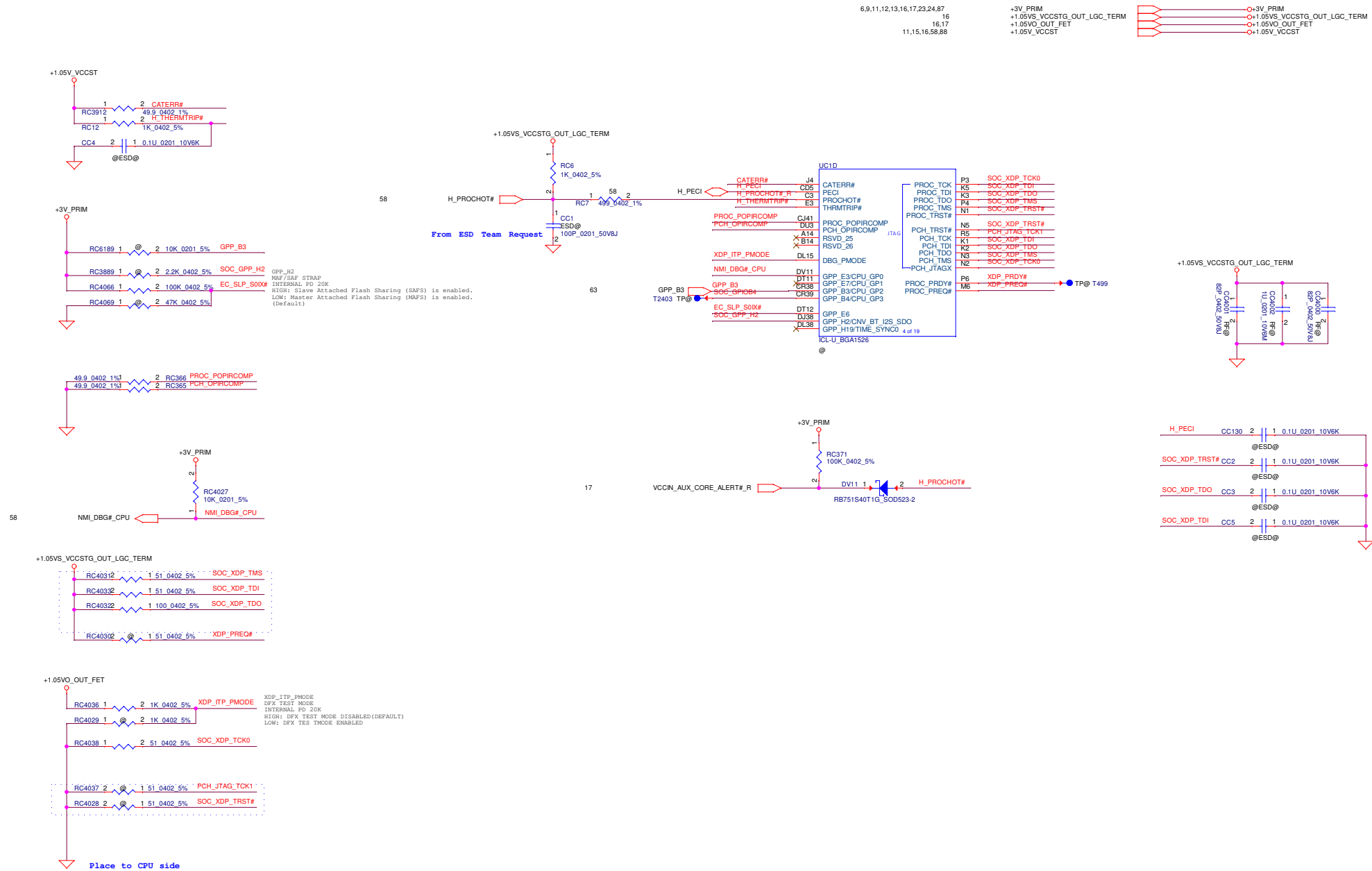


Table 5-11. USB2/USB2 Port Pairing for USB Type-C Connectors

	Connector C0	Connector C1	Connector C2	Connector C3
CPU USB3 port#	1	2	3	4
PCH USB2 port#	2	3	4	6

To make split xDCI controller working functionally for different USB-C connectors with increasing port numbers (TCP0_*, TCP1_*, TCP2_*, TCP3_*), recommended to pair with increasing number of USB2 ports from PCH. Simplest form of requirement is to match USB2/USB3 port numbers for USB-C connectors, but it is not strictly required.



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DDR4: Refer to 575034_ICL_U42_DDR4_T3_6L_Core_Schematics_Rev0p7

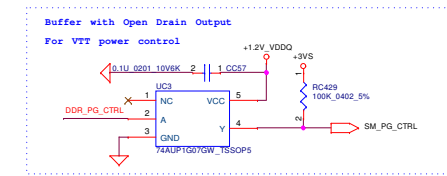
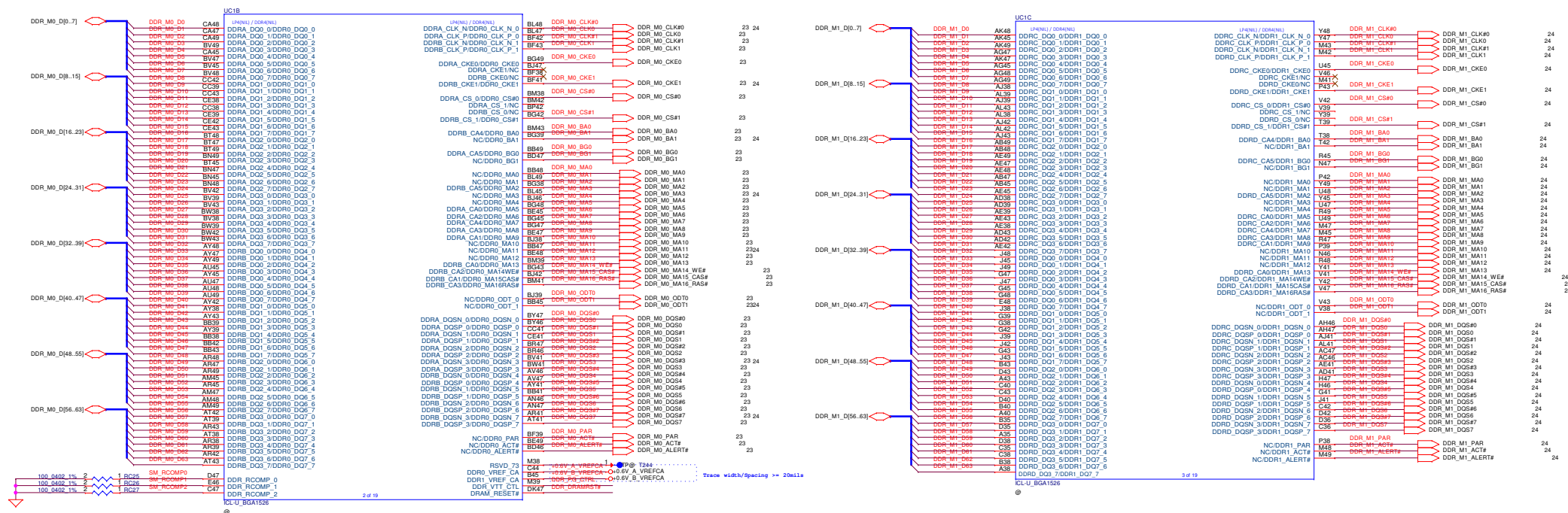
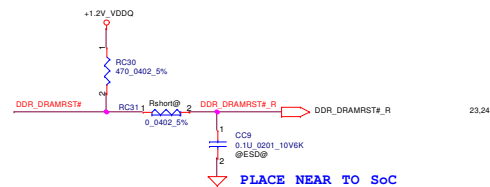
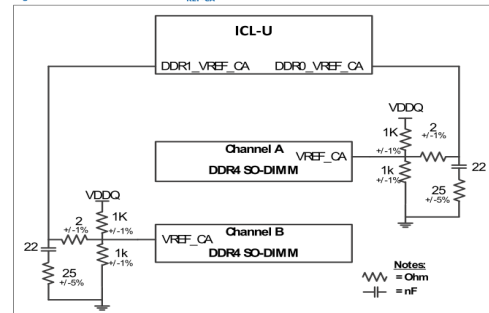
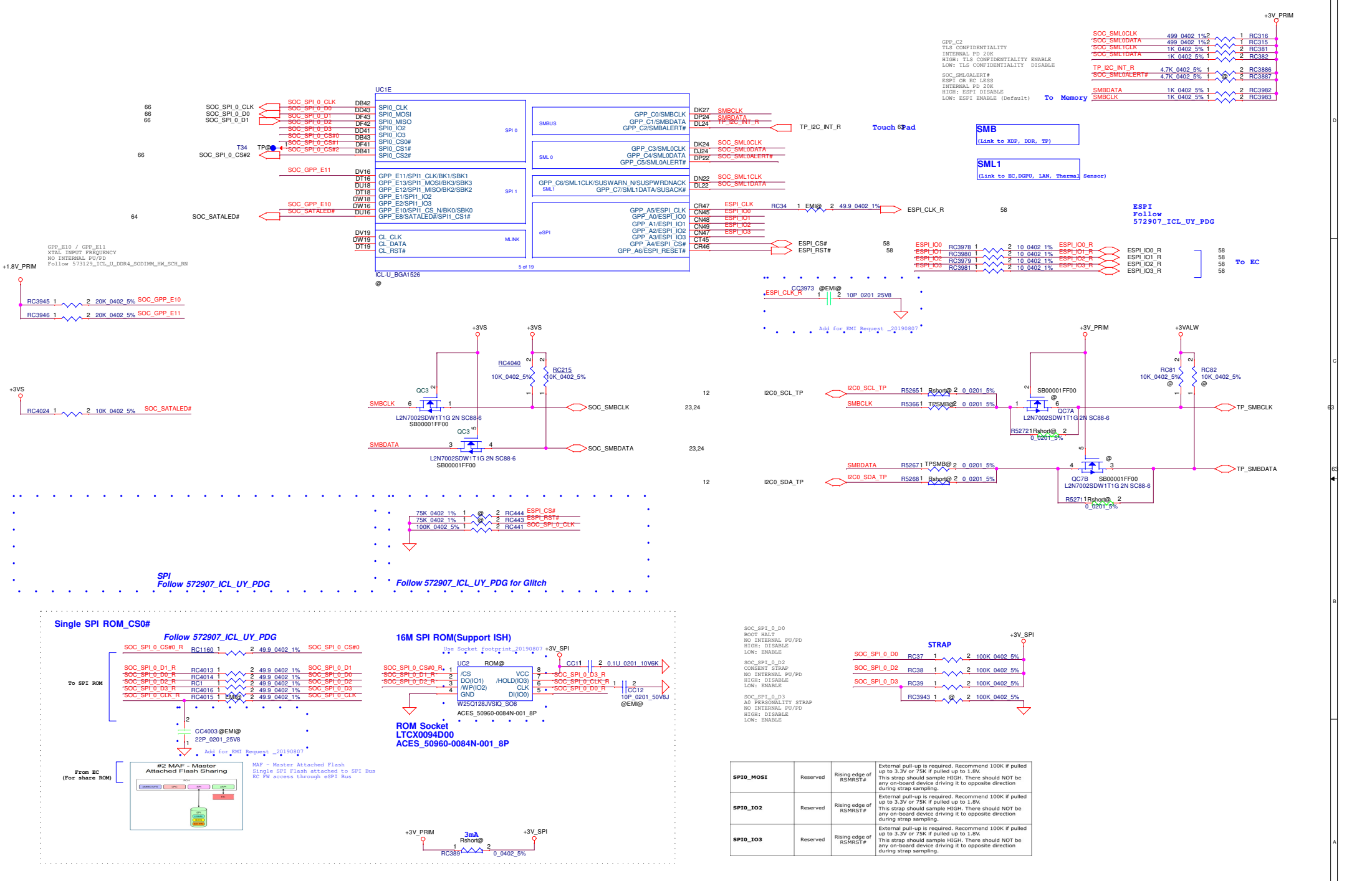


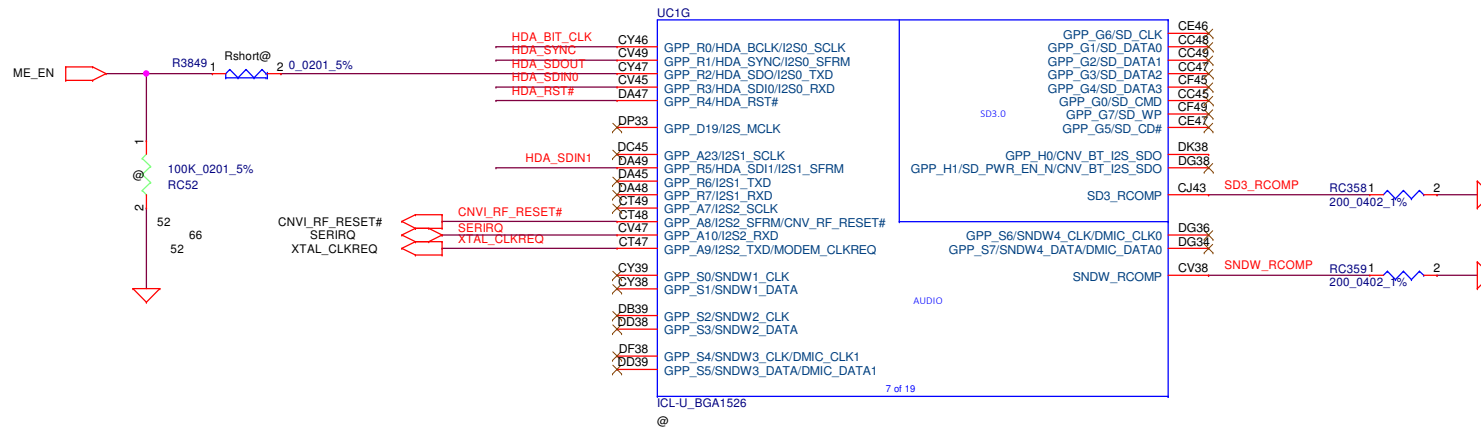
Figure 4-13. ICLU DDR4 SODIMM V_{REF-CA} Overview



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HDA_SDOUT
FLASH_DESCRIPTOR SECURITY OVERRIDE
INTERNAL PD 20K
HIGH: OVERRIDDEN
LOW: SECURITY MEASURES NOT OVERRIDDEN

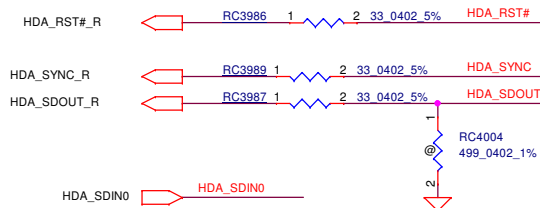
To Enable ME Override

572631_ICL_PCH_LP_EDS_Vol_1_Rev_0p7
VCCPGPPR: Audio Power 3.3V, 1.8V, or 1.5V
Need to sync with codec VDDIO

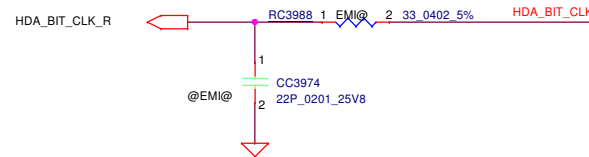
VGS(Max) : 1.0 V

Add for EMI Request _20190806

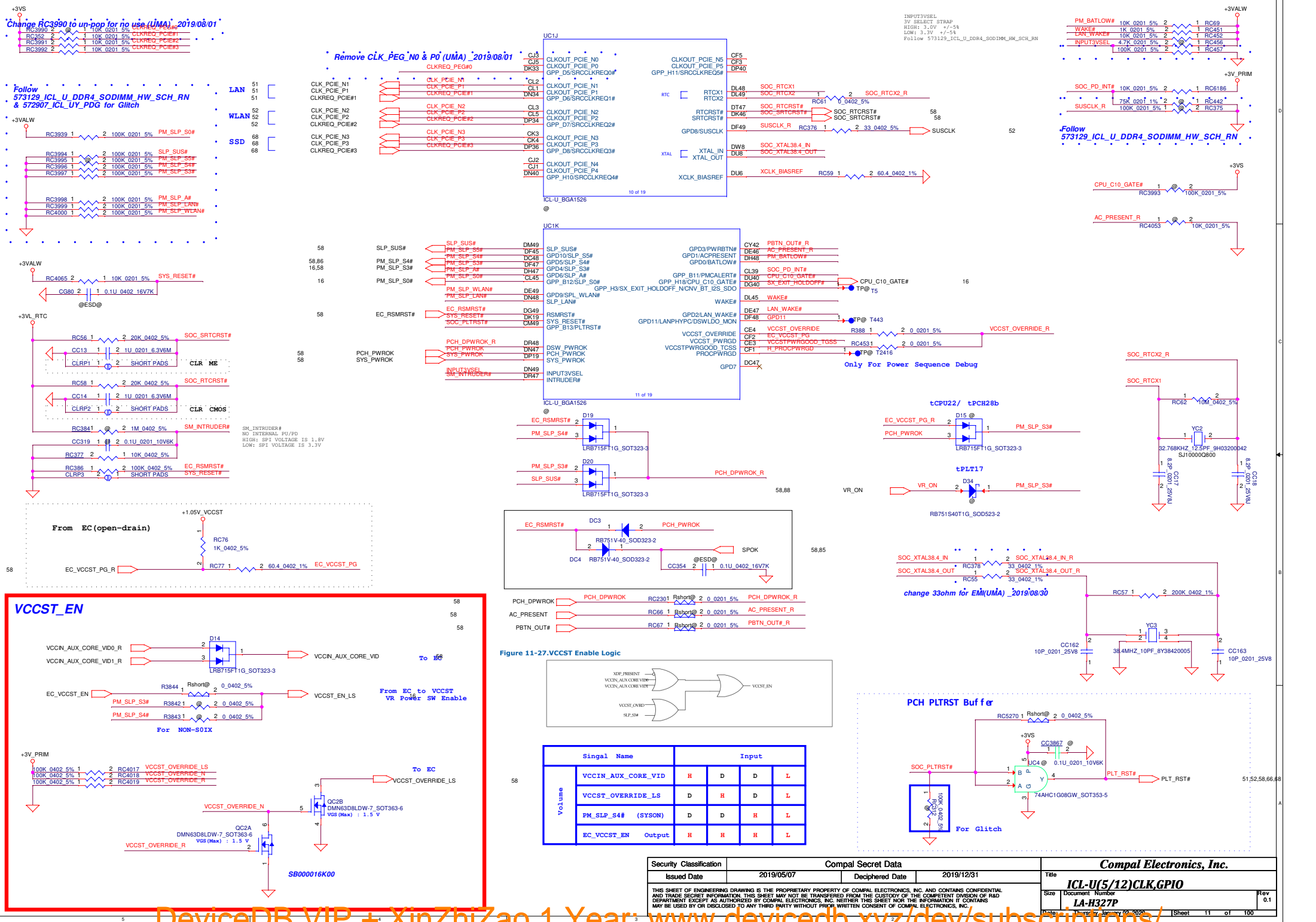
< HD AUDIO >

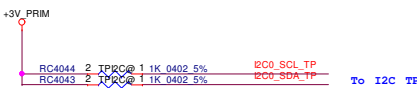
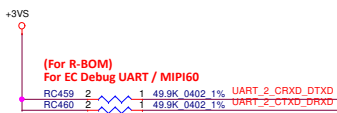


Follow
572907_ICL_UY_PDG for Glitch

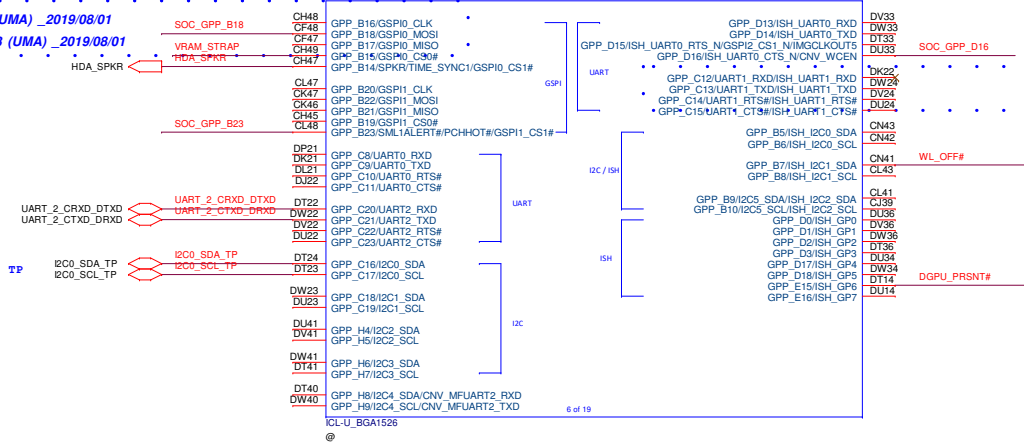


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										Rev 0.1	





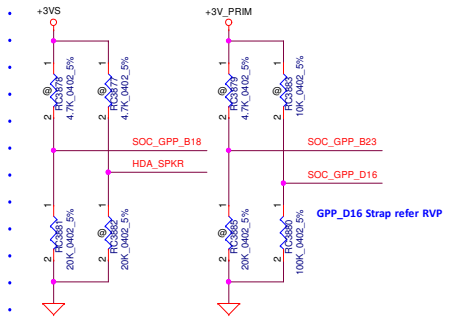
Remove GPU_EVENT# (UMA) _2019/08/01
Remove GC6_FB_ENV3 (UMA) _2019/08/01



Remove DGPU_PWR_EN PU to +3VS (UMA) _2019/08/02

Remove DGPU_HOLD_RST# (UMA) _2019/08/01
Remove DGPU_PWR_EN (UMA) _2019/08/02
Remove GPU_ALL_PGOOD (UMA) _2019/08/01

Strap Pin



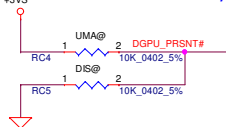
GPP_B23
CPUNSSC CLOCK FREQ
INTERNAL PD 20K
HIGH: 19.2 Mhz (form internal divider)
LOW: 38.4 Mhz (direct form crystal) (Default)

GPP_B18
No Reboot
INTERNAL PD 20K
HIGH: No Reboot
LOW: Reboot Enable (Default)

SPP2
TOP SWAP OVERRIDE
INTERNAL PD 20K
HIGH: Top swap enable
LOW: Disable (Default)

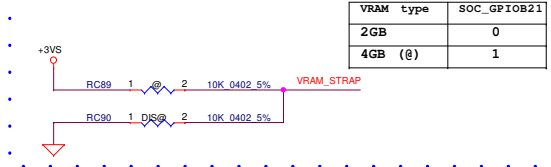
GPP_D16
NPU_MODE_DET_STRAP
Follow 573129_ICL-U_DDR4_SODIMM_HW_SCH_RN_IP0

For BIOS Verify UMA/DIS SKU



GPP_E15	DGPU_PRSNT#
DIS, Optimus	0
UMA	1

VRAM Strap Pin

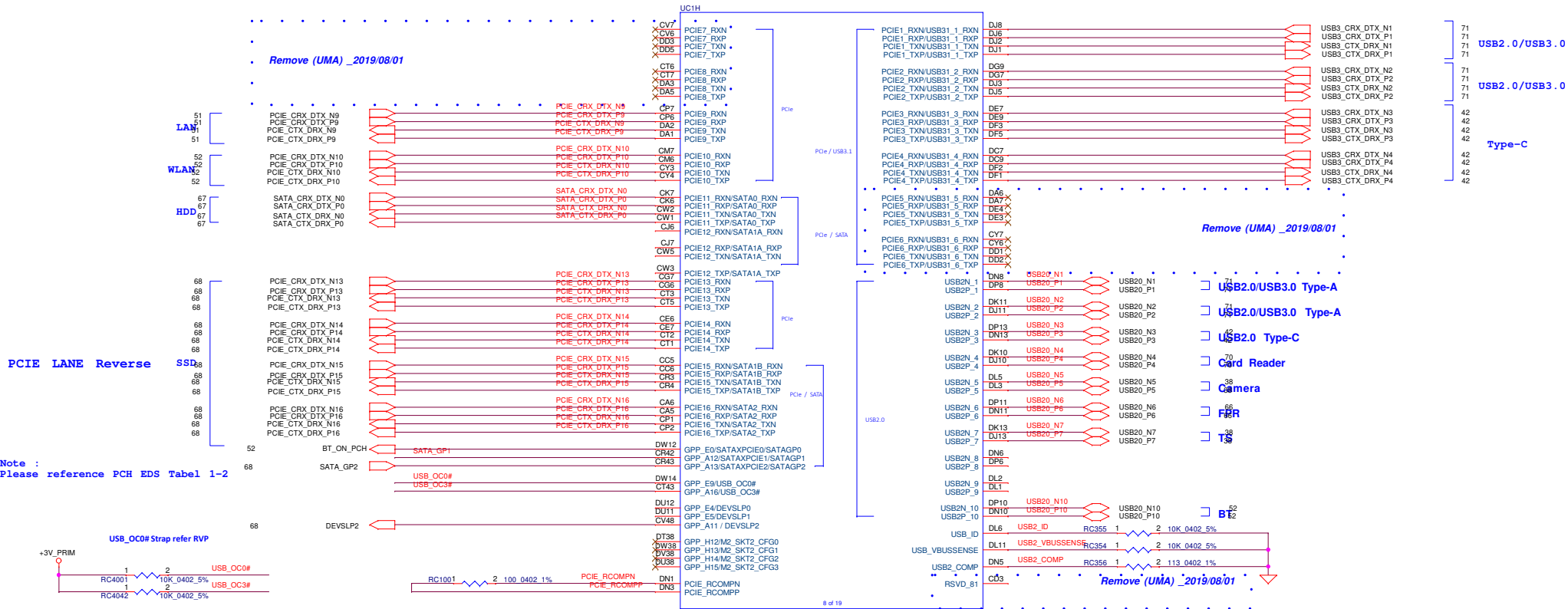


VRAM type	SOC_GP10B21
2GB	0
4GB (E)	1

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Device Gen1/2 need to check for 100nF
Gen3 for 220nF

Device Gen1/2 need to check for 100nF
Gen3 for 220nF



Note :
Please reference PCH EDS Table 1-2

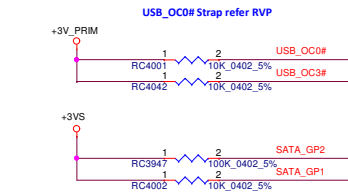


Table 6-24. SATA / PCI Express* Gen 2 and Gen 3 Capacitor Values

Condition	PCI Express* Gen 2 Only	PCI Express* Gen 3 Only	SATA Only	PCI Express* Gen 2/ SATA	PCI Express* Gen 3/ SATA
Processor Tx	100 nF	220 nF	10 nF	100 nF	220 nF
Processor Rx	None	None	10 nF	None	None

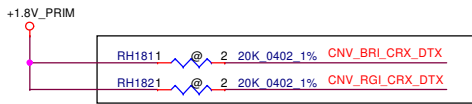
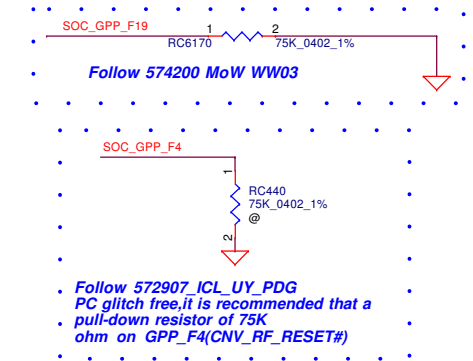
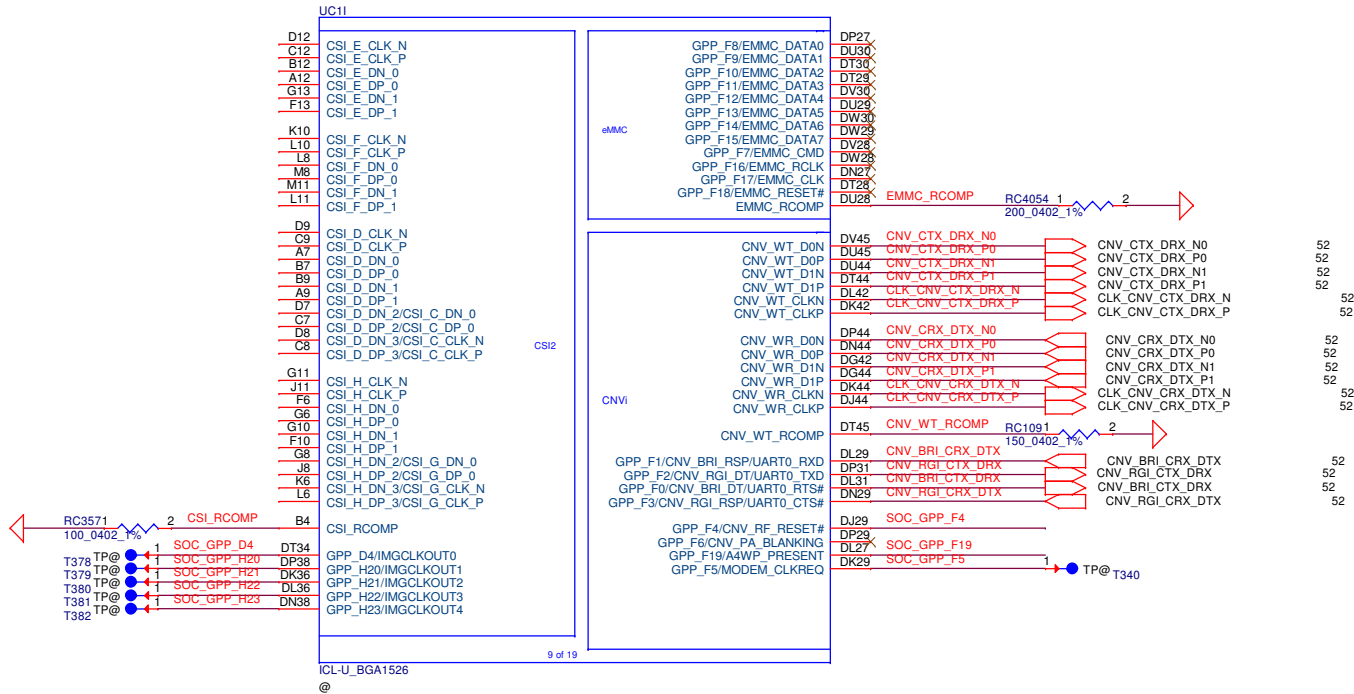
Notes:

- This option supports all SATA devices. However, the Rx 10 nF capacitor can be removed if DC coupled ODDs / Devices are NOT used.
- For PCIe* Gen 2/ SATA multiplexed configuration, motherboard Tx requires a 100 nF AC capacitor and NO AC capacitor is required for motherboard Rx channel. This option DOES NOT support DC coupled ODDs / Devices.
- For PCIe* Gen 3/ SATA multiplexed configuration, motherboard Tx requires a 220 nF AC capacitor and NO AC capacitor is required for motherboard Rx channel. This option DOES NOT support DC coupled ODDs / Devices.
- Design Constraint: For PCIe* lane that needs to support either PCIe* Gen2 devices or PCIe* Gen3 devices, follow the PCIe* Gen 3/ SATA multiplexed configuration, motherboard Tx requires a 220 nF AC capacitor and NO AC capacitor is required for motherboard Rx channel. This option DOES NOT support DC coupled ODDs / Devices.

Table 1-2. PCH HSIO Details

Flex I/O Lane	SKU		
	Premium U	Premium Y	Base U
0	USB3.1 Gen1/Gen2, PCIe*	USB3.1 Gen1/Gen2, PCIe*	USB3.1 Gen1
1	USB3.1 Gen1/Gen2, PCIe*	USB3.1 Gen1/Gen2, PCIe*	USB3.1 Gen1
2	USB3.1 Gen1/Gen2, PCIe*	USB3.1 Gen1/Gen2, PCIe*	USB3.1 Gen1
3	USB3.1 Gen1/Gen2, PCIe*	USB3.1 Gen1/Gen2, PCIe*	USB3.1 Gen1
4	USB3.1 Gen1/Gen2, PCIe*	USB3.1 Gen1/Gen2, PCIe*	PCIe*
5	USB3.1 Gen1/Gen2, PCIe*	USB3.1 Gen1/Gen2, PCIe*	PCIe*
6	PCIe*, GbE	PCIe*, GbE	PCIe*, GbE
7	PCIe*, GbE	PCIe*, GbE	PCIe*, GbE
8	PCIe*, GbE	PCIe*, GbE	PCIe*, GbE
9	PCIe*	PCIe*	PCIe*
10	PCIe*, SATA	PCIe*, SATA	PCIe*, SATA
11	PCIe*, SATA	PCIe*, SATA	PCIe*, SATA
12	PCIe*, GbE	PCIe*, GbE	PCIe*, GbE
13	PCIe*, GbE	PCIe*, GbE	PCIe*, GbE
14	PCIe*, SATA	NA	PCIe*
15	PCIe*, SATA	NA	PCIe*

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CNV_RGL_CTX_DRX

M.2 CNVi MODES

0 = Integrated CNVi enable.

1 = Integrated CNVi disable.

NO INTERNAL PU/PD

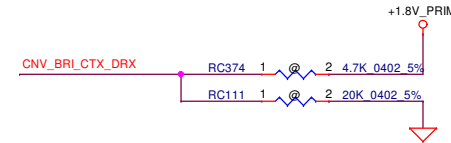
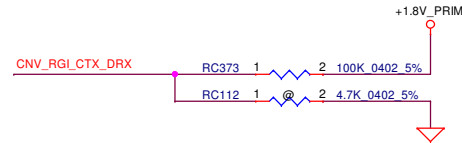
CNV_BRI_CTX_DRX

XTAL SEL

0 = 38.4/19.2MHZ (DEFAULT)

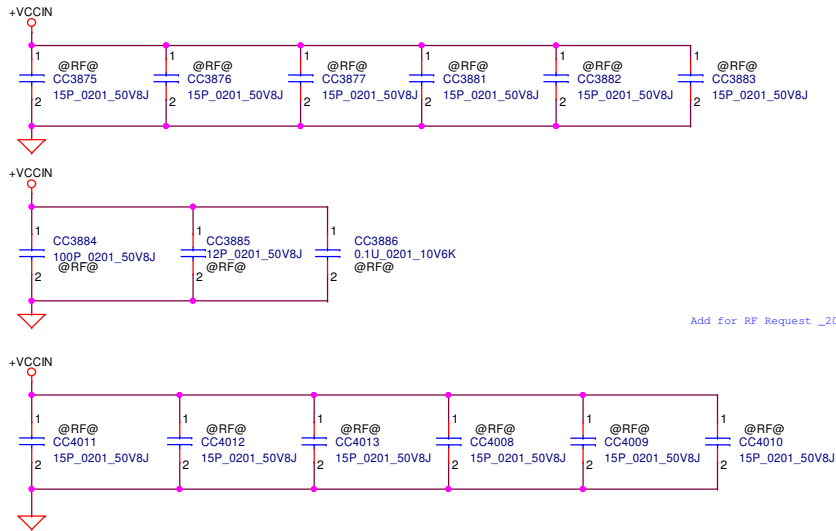
1 = 24MHZ (25 MHZ WHEN XTAL FREQ DIVIDER NON ZERO)

WEAK INTERNAL PD 20K



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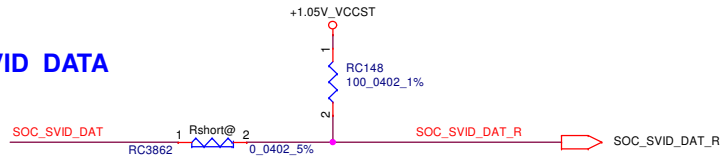
FIVR Decoupling Caps -PLACE < 5mm from SOC VCCIN



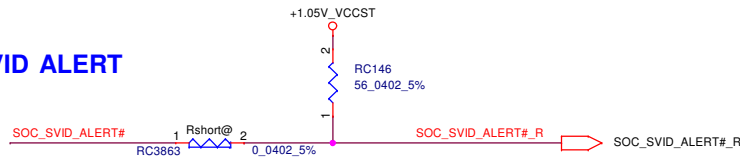
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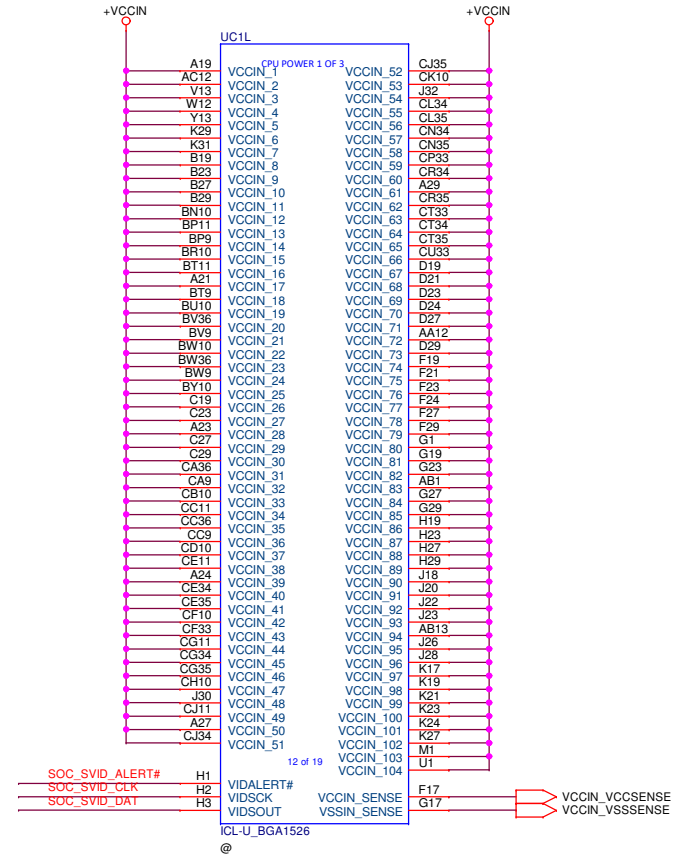
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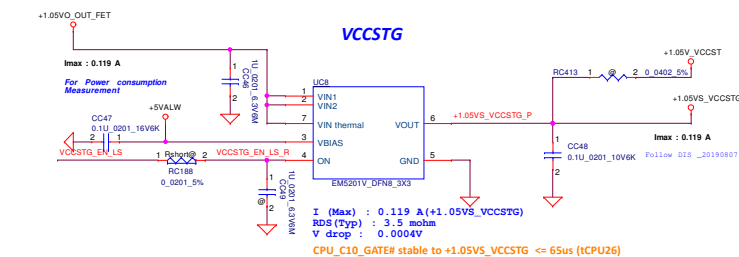
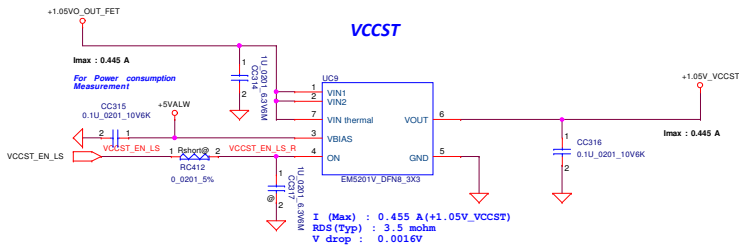
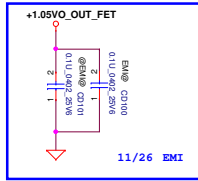
SVID ALERT



SVID CLOCK



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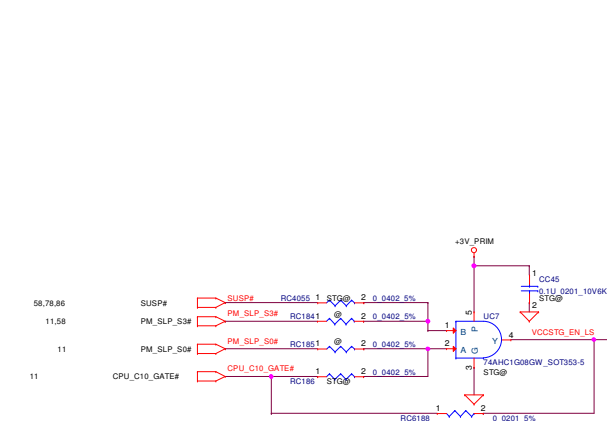


For NON-S0IX

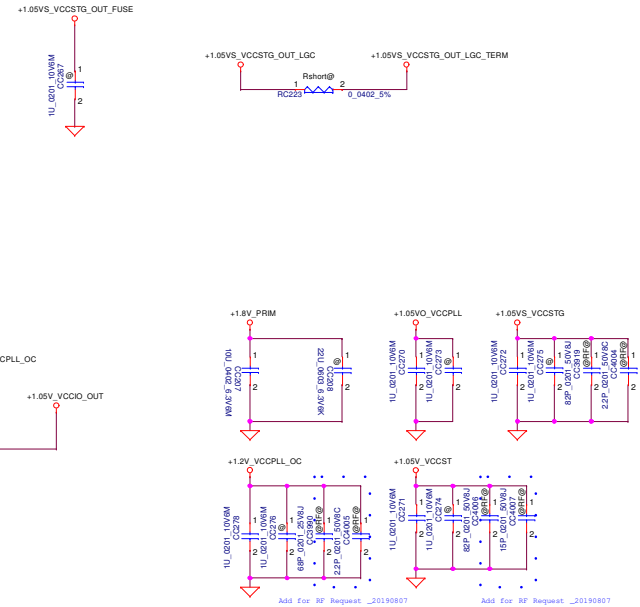
$+1.2V_VDDQ$ $+1.2V_VCCPLL_OC$

RC254 1 2 0.0402 5%

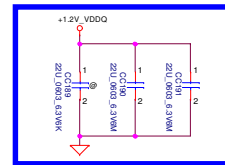
$I_{max} : 0.152\text{ A}$

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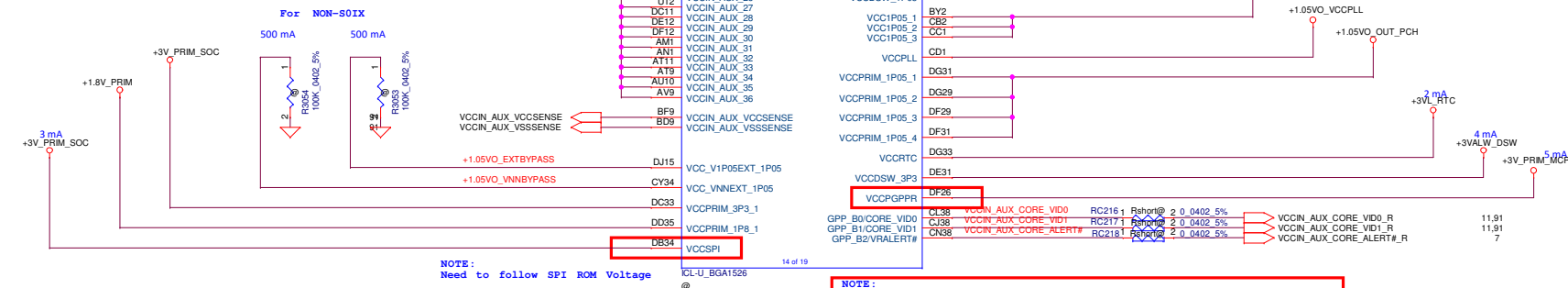
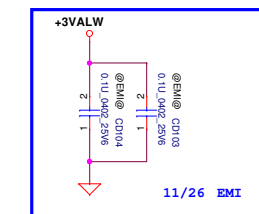
Volume	Premium
VccSTG and VccST are merged and gated by SLP_S4#	VccSTG gated by {CPU_C10_GATE#}
VccPLL_OC is supplied directly from VDDQ	VccPLL_OC is supplied from VDDQ through a load switch
VCC1P8A on the CPU is supplied directly by V1.8A	VCC1P8A is supplied from V1.8A and gated by CPU_C10_GATE #
VCC_VNNEXT_1P05 is not used	VCC_VNNEXT_1P05 is supplied by small dedicated VNR VR to bypass PCH FIVR during light load
VCC_V1P05EXT_1P05 is not used	VCC_V1P05EXT_1P05 is supplied by small dedicated V1_05A VR to bypass PCH FIVR during light load
Various system devices share load switches	Various system devices have their own independent load switches



Place on CPU Side
22uF* 2 + 22uF* 1 (Reserved)



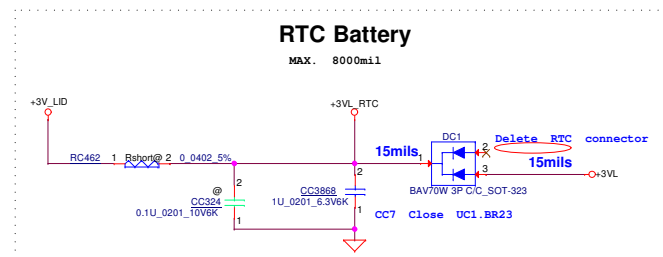
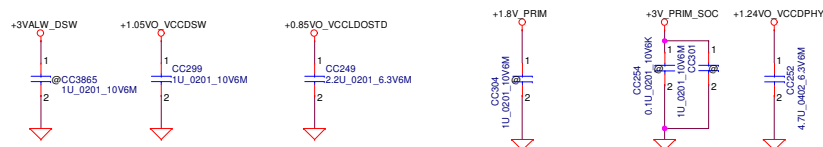
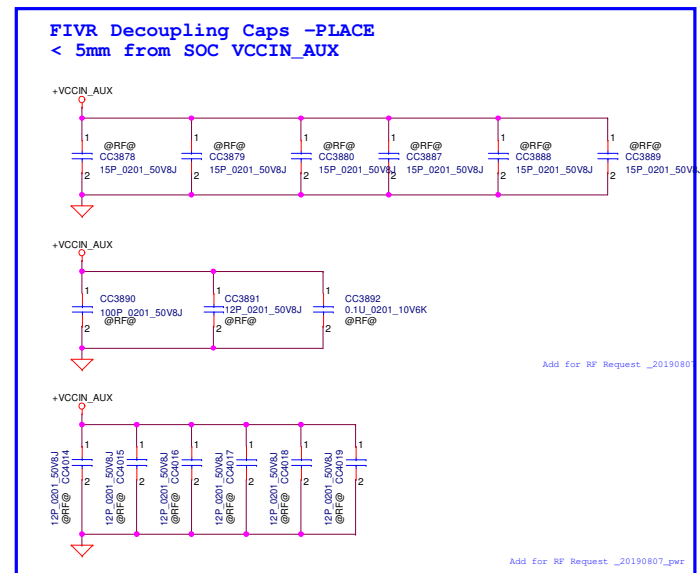
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				LA-H327P			
				Date:	Wednesday, January 08, 2020	Sheet	16



NOTE:
Need to follow SPI ROM Voltage

```
NOTE:
572631_ICL_PCH_LP_EDS_Vol_1_Rev_1p0
VCCPGPPR: Audio Power 3.3V, 1.8V, or 1.5V
Need to sync with codec VDDIO.

572907_ICL_UY_PDG_Rev1p1
When configured as 3.3V or 1.8V, VCCPGPPR can be merged directly with
either VCCPRIM1_P8 or VCCPRIM1_P3 depending on their operating voltage.
```



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				ICL-U(11/13)Power Size Document Number LA-H327P	
Date: Thursday, January 02, 2020				Sheet 17 of 100	

UC10		
GND 1 OF 3		
A11	VSS_1	AF45
A46	VSS_2	AF47
BA45	VSS_3	AG1
BA47	VSS_7	AG11
BB11	VSS_4	AG3
BB3	VSS_5	AG38
BB7	VSS_6	AG39
BC37	VSS_8	AG41
BD3	VSS_9	AG42
BD38	VSS_10	AG43
BD41	VSS_11	AG5
BD43	VSS_12	AG6
A48	VSS_13	AG9
BD42	VSS_14	AH2
BD43	VSS_15	AH37
BD45	VSS_16	AH45
BD49	VSS_17	AH49
BD5	VSS_18	AJ2
BD6	VSS_19	AJ3
BD7	VSS_20	AJ4
BE1	VSS_21	AK37
BE2	VSS_22	AL2
BF3	VSS_23	AL45
A49	VSS_24	AL47
BF45	VSS_25	AL6
BF47	VSS_26	AM2
BF7	VSS_27	AM37
BG3	VSS_28	AM38
BG41	VSS_29	AN38
BG7	VSS_30	AN39
BH37	VSS_31	A36
BJ1	VSS_32	AN41
BJ2	VSS_33	AN42
BJ3	VSS_34	AN43
AA45	VSS_35	AN45
BJ41	VSS_36	AN49
BJ43	VSS_37	AN6
BJ45	VSS_38	AR1
BJ49	VSS_39	AR11
BJ7	VSS_40	AR2
BM11	VSS_41	AR3
BM3	VSS_42	A39
BM45	VSS_43	AR7
BM47	VSS_44	AR9
BM5	VSS_45	AT3
AA47	VSS_46	AT45
BM6	VSS_47	AT47
BM7	VSS_48	AT5
BP1	VSS_49	CG37
BP2	VSS_50	AT7
BP3	VSS_51	AU37
BP43	VSS_52	AV11
BP7	VSS_53	A42
BR45	VSS_54	AV3
BR49	VSS_55	AV38
AB11	VSS_56	AV39
AB3	VSS_57	AV41
AB38	VSS_58	AV42
AB39	VSS_59	AV43
AB41	VSS_60	AV45
A17	VSS_61	AV49
AB42	VSS_62	AV7
AB43	VSS_63	AY3
AB5	VSS_64	A44
AB6	VSS_65	AY7
AC45	VSS_66	B17
AC49	VSS_67	B21
AD10	VSS_68	B24
AD11	VSS_69	B2
AD34	VSS_70	B3
AD37	VSS_71	B31
A3	VSS_72	B48
AE6	VSS_73	BA1
AF37	VSS_74	BA2

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ICL-U_BGA1526

@

UC1P		
GND 2 OF 3		
BT3	VSS_149	CR37
BT39	VSS_150	CR45
BT41	VSS_151	CR49
BT42	VSS_152	CT37
BT43	VSS_153	CT39
BT7	VSS_154	CT42
BU45	VSS_155	CT9
BU47	VSS_156	CU45
BV1	VSS_157	CU47
BV11	VSS_158	CU49
BV2	VSS_159	CV3
BV3	VSS_160	CV34
BV7	VSS_161	CV35
BW3	VSS_162	CV5
BW37	VSS_163	CV9
BW5	VSS_164	CY41
BW6	VSS_165	CY45
BW7	VSS_166	CY49
BY37	VSS_167	CY9
BY45	VSS_168	D1
BY49	VSS_169	D17
C11	VSS_170	D31
C13	VSS_171	D44
C14	VSS_172	D49
C17	VSS_173	DA10
C21	VSS_174	DA33
C24	VSS_175	DA9
C31	VSS_176	DB32
C34	VSS_177	DB35
C39	VSS_178	DB38
C48	VSS_179	DB45
C49	VSS_180	DB47
C6	VSS_181	DB49
CA3	VSS_182	DC3
CA38	VSS_183	DC49
CA41	VSS_184	DC5
CA42	VSS_185	DC6
CA43	VSS_186	DD37
CA7	VSS_187	DD42
CB37	VSS_188	DE10
CB45	VSS_189	DE13
CB47	VSS_190	DE17
CC3	VSS_191	DE18
CC7	VSS_192	DE20
CE37	VSS_193	DE22
CE45	VSS_194	DE23
CE49	VSS_195	DE26
CE9	VSS_196	DE28
CG37	VSS_197	DE29
CG39	VSS_198	DE33
CG43	VSS_199	DE45
CG45	VSS_200	DE6
CG47	VSS_201	DF13
CH3	VSS_202	DF22
CH5	VSS_203	DF28
CJ37	VSS_204	DF33
CJ42	VSS_205	DF35
CJ9	VSS_206	DF39
CK45	VSS_207	DG10
CK49	VSS_208	DG12
CK9	VSS_209	DG13
CL37	VSS_210	DG15
CL42	VSS_211	DG22
CL49	VSS_212	DG23
CM45	VSS_213	DG26
CM47	VSS_214	DG47
CM9	VSS_215	DH1
CN3	VSS_216	DH45
CN37	VSS_217	DH5
CN39	VSS_218	DJ19
CN5	VSS_219	DJ21
CP9	VSS_220	DJ27
CR32	VSS_221	DJ31
	VSS_222	

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ICL-U_BGA1526

@

UC1Q		
GND 3 OF 3		
DJ33	VSS_297	F11
DJ36	VSS_298	F31
DJ42	VSS_299	F45
DK3	VSS_300	F47
DK4	VSS_301	F8
DK49	VSS_302	G21
DK6	VSS_303	G24
DK8	VSS_304	G3
DL10	VSS_305	G31
DL13	VSS_306	G36
DL44	VSS_307	G49
DL47	VSS_308	G5
DM47	VSS_309	H17
DN15	VSS_310	H21
DN19	VSS_311	H24
DN24	VSS_312	H31
DN31	VSS_313	H33
DN36	VSS_314	H36
DN42	VSS_315	H45
DP45	VSS_316	H49
DR49	VSS_317	J10
DT1	VSS_318	J13
DT10	VSS_319	J16
DT15	VSS_320	J36
DT20	VSS_321	J6
DT27	VSS_322	K11
DT3	VSS_323	K33
DT32	VSS_324	K8
DT37	VSS_325	L36
DT42	VSS_326	L39
DT49	VSS_327	L41
DT6	VSS_328	L42
DT7	VSS_329	L43
DT8	VSS_330	L45
DU1	VSS_331	L47
DU10	VSS_332	M10
DU15	VSS_333	M3
DU2	VSS_334	M36
DU20	VSS_335	M5
DU27	VSS_336	N45
DU32	VSS_337	N49
DU37	VSS_338	P11
DU48	VSS_339	P41
DU49	VSS_340	P8
DU7	VSS_341	R3
DV2	VSS_342	R37
DV44	VSS_343	T11
DV48	VSS_344	T36
DV8	VSS_345	T41
DW1	VSS_346	T43
DW10	VSS_347	T45
DW2	VSS_348	T47
DW20	VSS_349	U3
DW27	VSS_350	U37
DW44	VSS_351	U5
DW46	VSS_352	V11
DW48	VSS_353	V36
DW49	VSS_354	V45
DW7	VSS_355	V49
E11	VSS_356	V9
E34	VSS_357	W37
E36	VSS_358	Y36
E39	VSS_359	Y38
E42	VSS_360	Y43
E6	VSS_361	Y9
		DE15

17 of 19

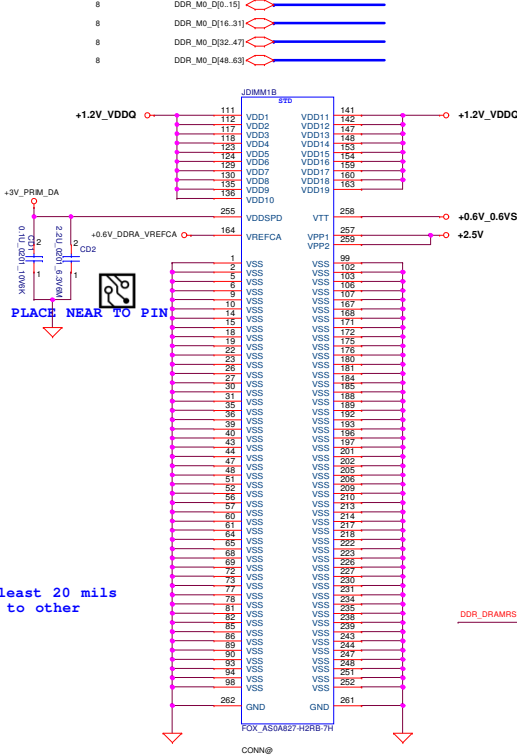
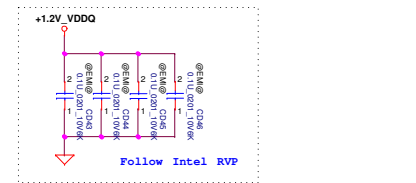
ICL-U_BGA1526

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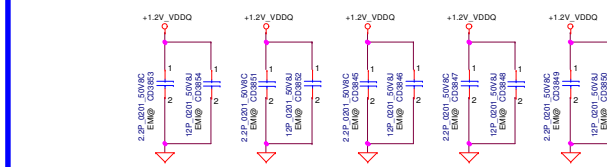
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					LA-H327P	
				Drawn By	Checked By	Sheet 18 of 100

REVERSE TYPE

Non-Interleaved Memory

[illegible]

EMC CAPS-PLACE
< 4mm from SO-DIMM VDDQ
with each pair < 12mm Apart
12pF* 5 (EMI@)
2.2pF* 5 (EMI@)



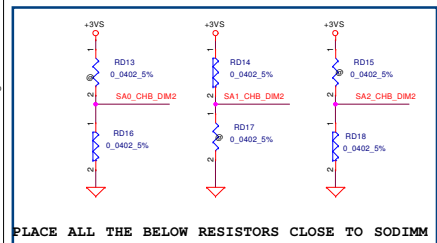
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MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPTEL ELECTRONICS, INC.			Date: Thursday, January 02, 2020 Sheet 23 of 100	

CHANNEL-M1

TOP: JDIMM2 CONN Non-ECC DIMM

Non-Interleaved Memory

STD (5.2 mm)



SPD ADDRESS FOR CHANNEL B :

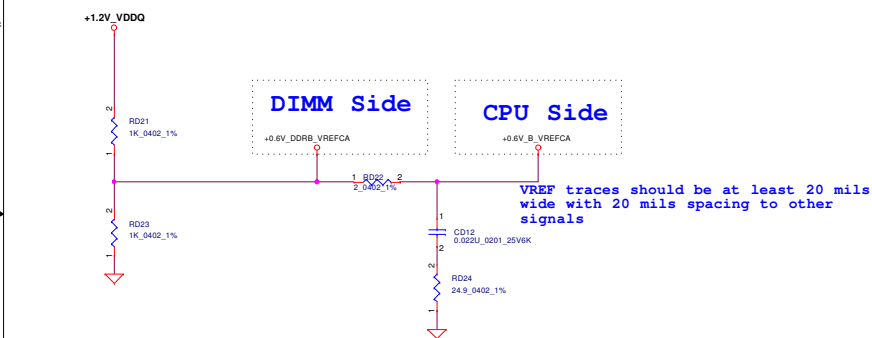
WRITE ADDRESS: 0XA4

READ ADDRESS: 0XA3

SA0 = 0; SA1 = 1; SA2 = 0.

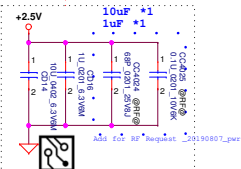
DDR4 POR OPERATING SPEED: 1867 MT/S

STRETCH GOAL IS 2133 MT/S

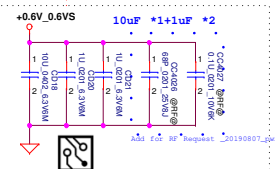


Decoupling Cap_Channel B

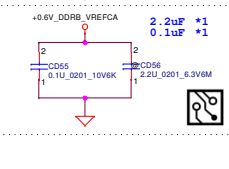
Layout Note:
Place near JDIMM1.257,259



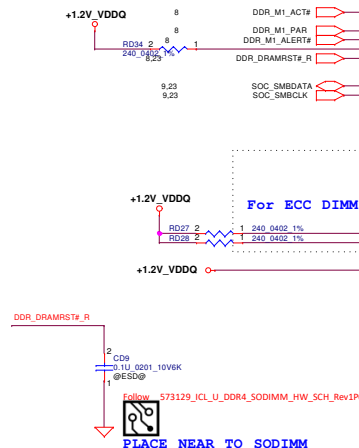
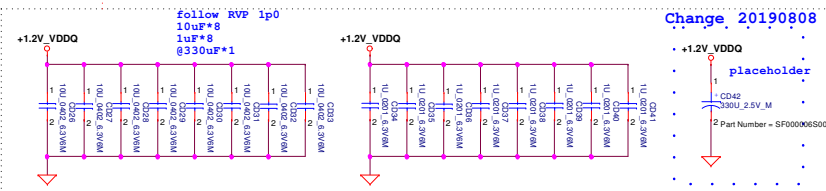
Layout Note:
Place near JDIMM1.258



Layout Note:
Place near JDIMM1.258



Layout Note:
Place near JDIMM1



Update Table 4-26 For DDR4 SODIMM Decoupling Caps
572907_ICL_UY_PbG_Rev07

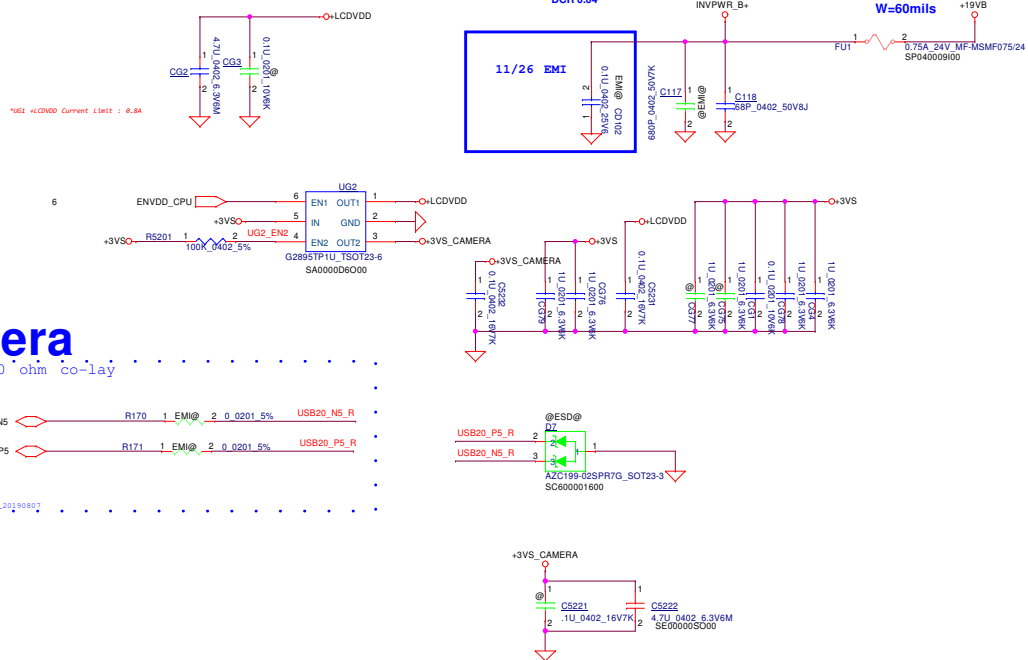
Table 4-26. DDR4 SODIMM Power Plane Decoupling

Memory Configuration	Power Domain	Decoupling Location	Qty x uF (size)
DDR4 SODIMM 1DCP	VDDQ/VDD	4 near each side of the DIMM connector close to VDD pins	16x 10uF (0603)
		4 near each side of the DIMM connector close to VDD pins	16x 1uF (0402)
	VTT	Place on VTT plane close to DIMM	1x 330uF (7343)
		1 cap stuffed, 1 placeholder	2x 10uF (0603)
	VPP	Place on VTT plane close to DIMM	4x 1uF (0402)
		DIMM pin side, 1 per DIMM	2x 10uF (0603)
VDDSPD		DIMM pin side, 1 per DIMM	2x 1uF (0402)
		Place close to DIMM	2x 0.1uF (0402)
VDDSPD		Place close to DIMM	2x 2.2uF (0402)
		Place close to DIMM	2x 2.2uF (0402)

Note:
1. Total quantity is referring to 2 channels.

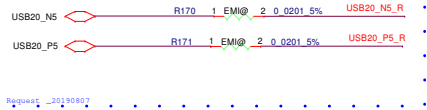
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Issued Date	2019/05/07	Deciphered Date	2019/12/31	Title	
				DDR4 CHM1: DIMM1	
				Rev 6.1	
				LA-H327P	
				Date: Thursday, January 02, 2020	
				Sheet 24 of 100	

eDP Power



Camera

Choke and 0 ohm co-lay



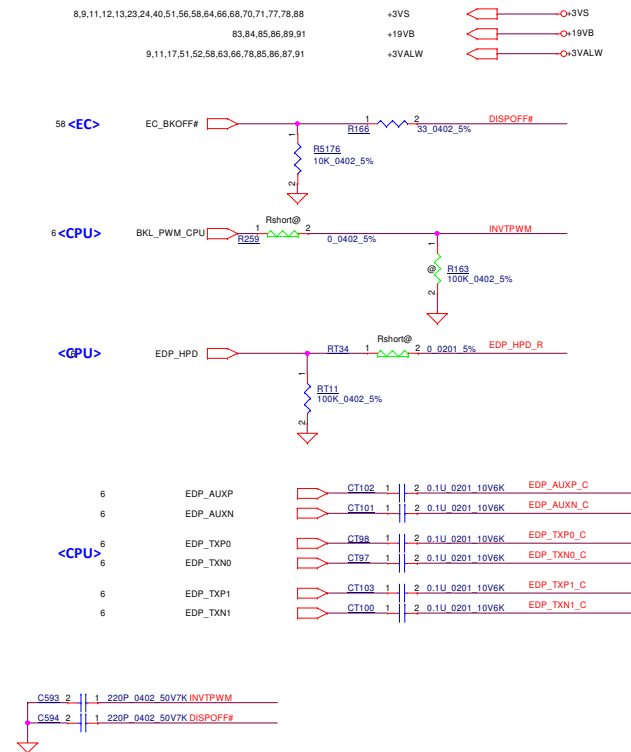
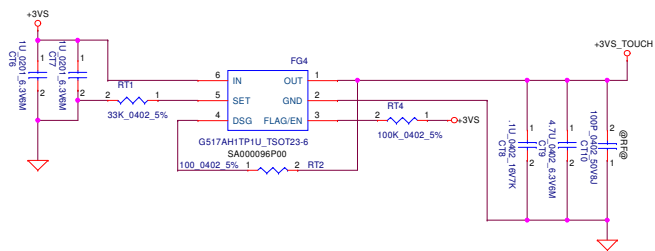
Add for ENI Request _20190807

Touch Screen

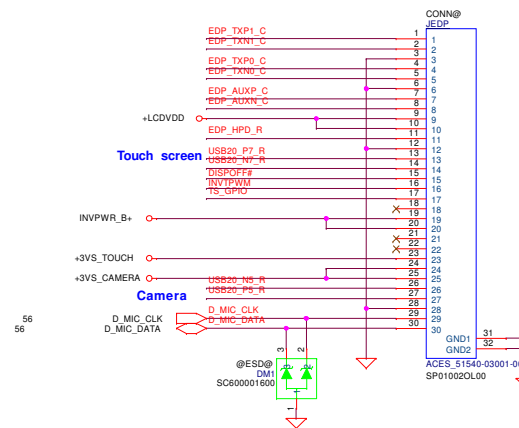
Choke and 0 ohm co-lay



Touch Screen Power Selection:



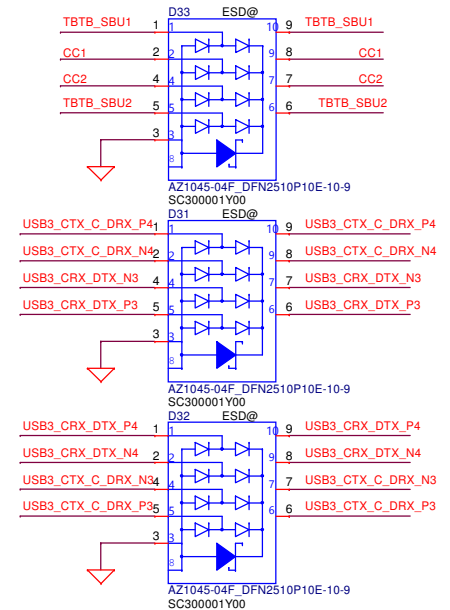
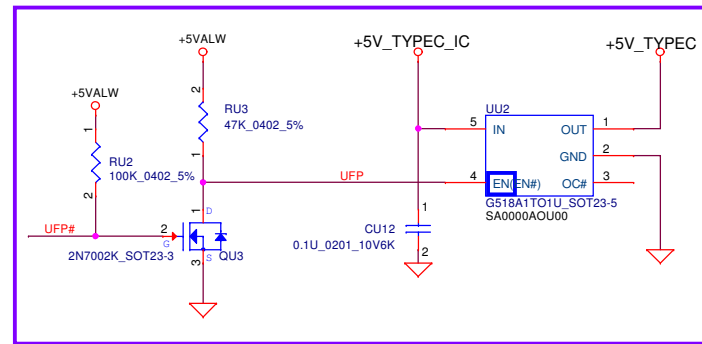
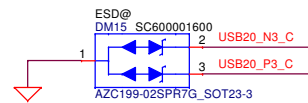
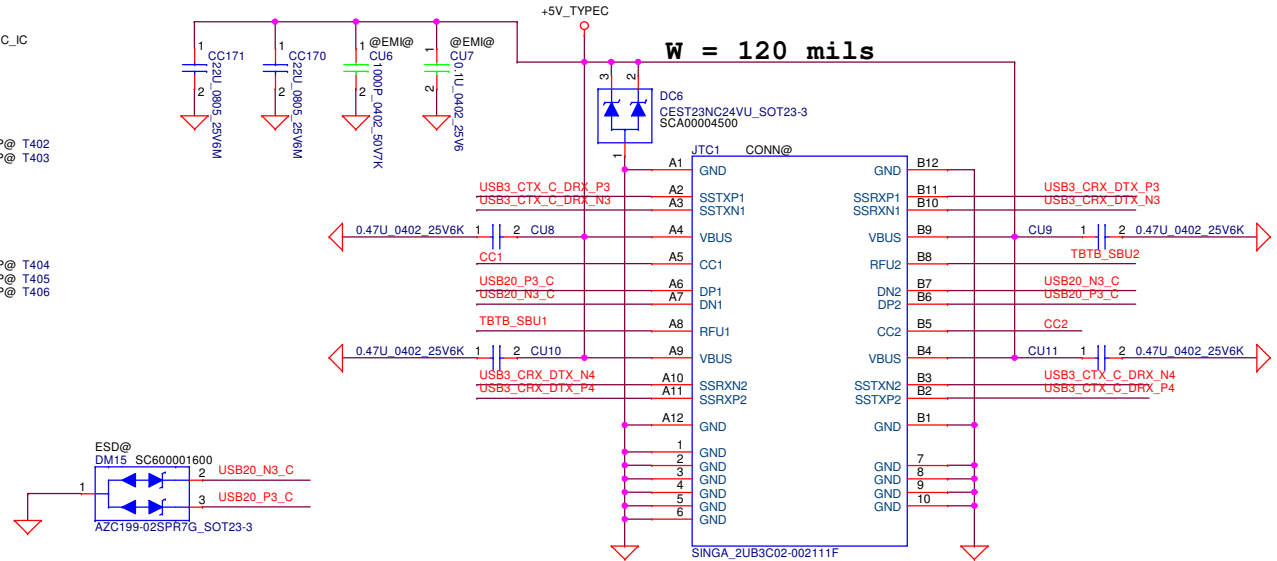
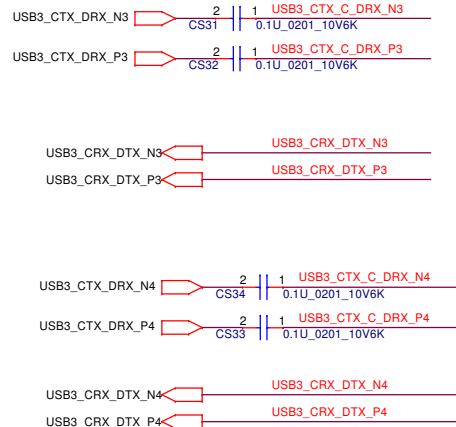
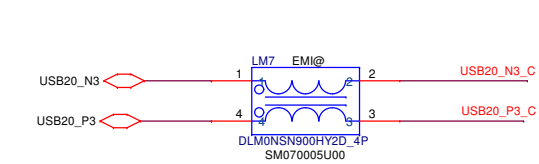
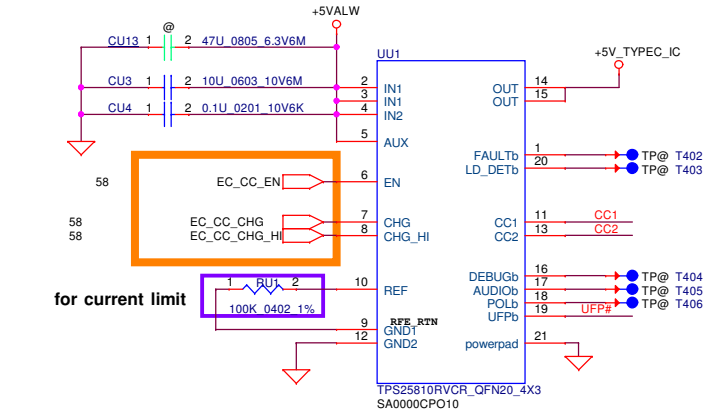
eDP



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					LA-H327P
				Date:	Wednesday, January 08, 2020
				Sheet	38 of 100



Type-C - USB only



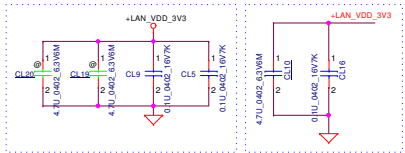
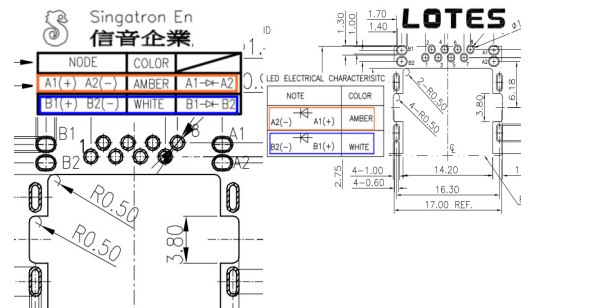
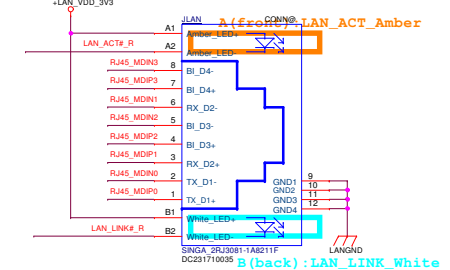
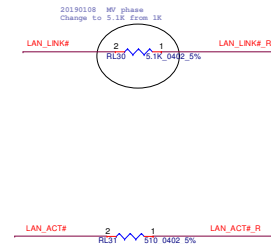
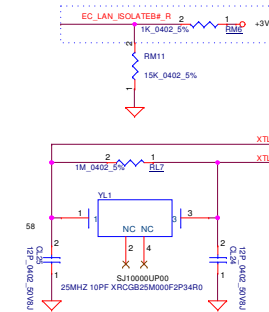
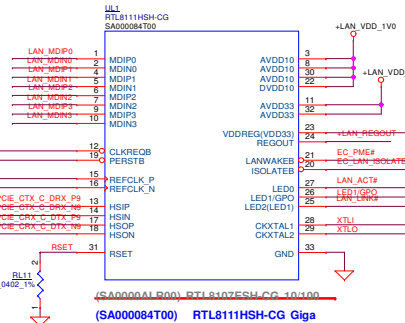
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						Type-C Conn				
						Size	Document Number			
						Customer	LA-H327P			
						Rev	0.1			
						Sheet 42 of 100				

+LAN_VDD_3V3 Rising time
need>0.5mS and
<100mS

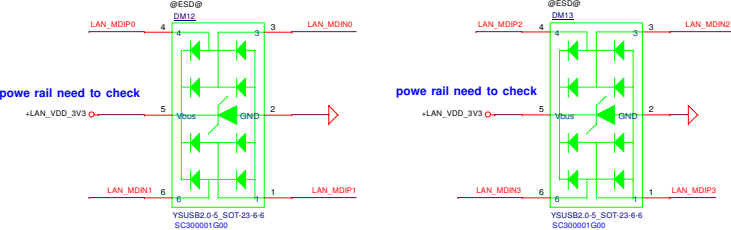
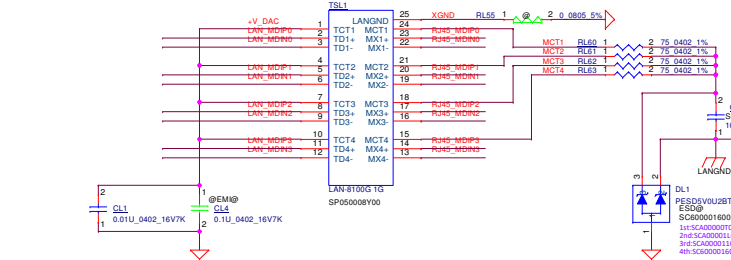
CL8, CL23 close LL2.
CL26 close UL1 Pin 3.
CL12 close UL1 Pin 8.
CL13 ~ CL15 close UL1 Pin 22.
CL11, CL27 close UL1 Pin 30.

RTL8107ESH-CG/RTL8111HSH-CG Co-Lay

+LAN_VDD_3V3=40mil
+VDDREG=40mil
+LAN_REGOUT=60mil



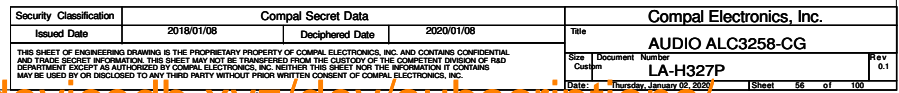
CL9, CL20 close to UL1 Pin 11
CL5 & CL19 close to UL1: Pin 32



power rail need to check

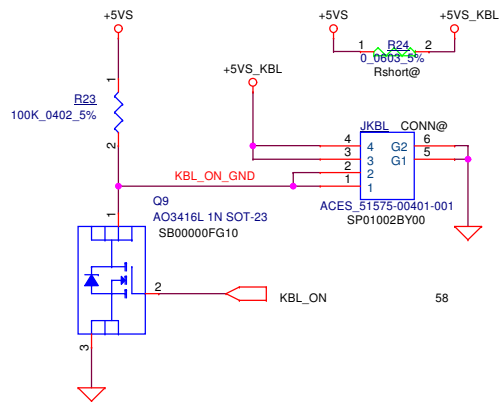
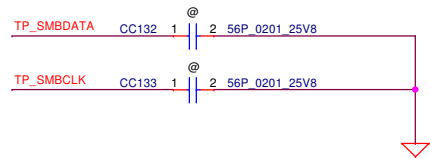
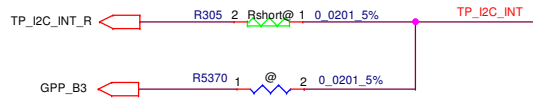
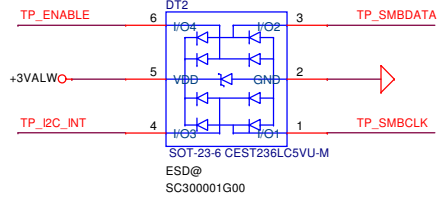
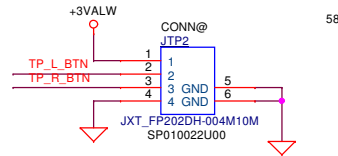
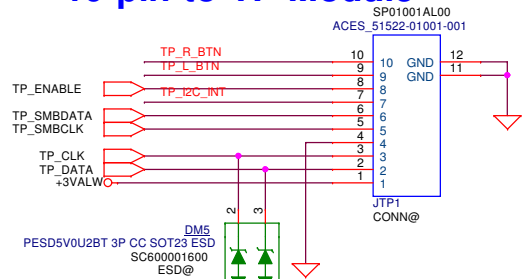
power rail need to check

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10 pin to TP Module

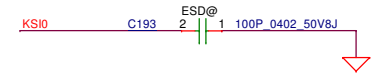
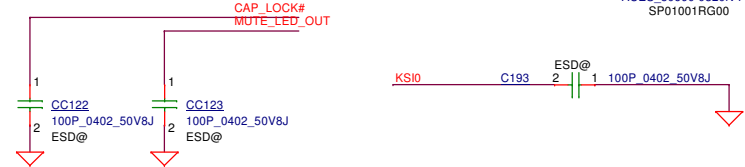
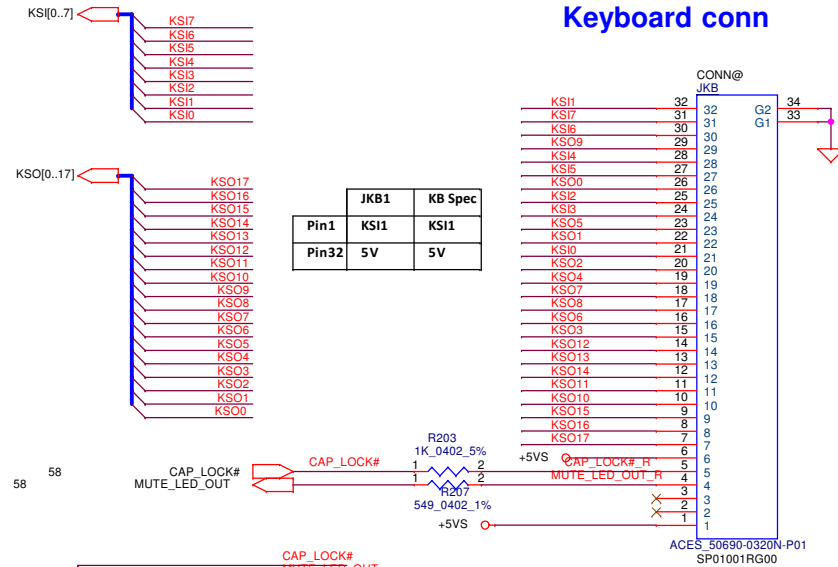
4 pin to TP S/B



9,11,17,51,52,58,66,78,85,86,87,91
16,42,64,71,78,85,86,88,89,91

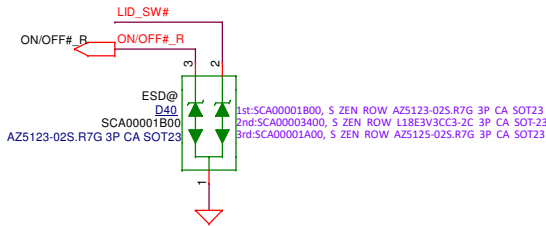
+3VALW
+5VALW

Keyboard conn

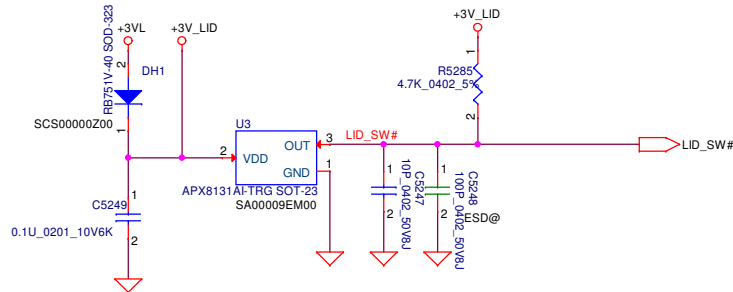


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				Date:	Thursday, January 02, 2020
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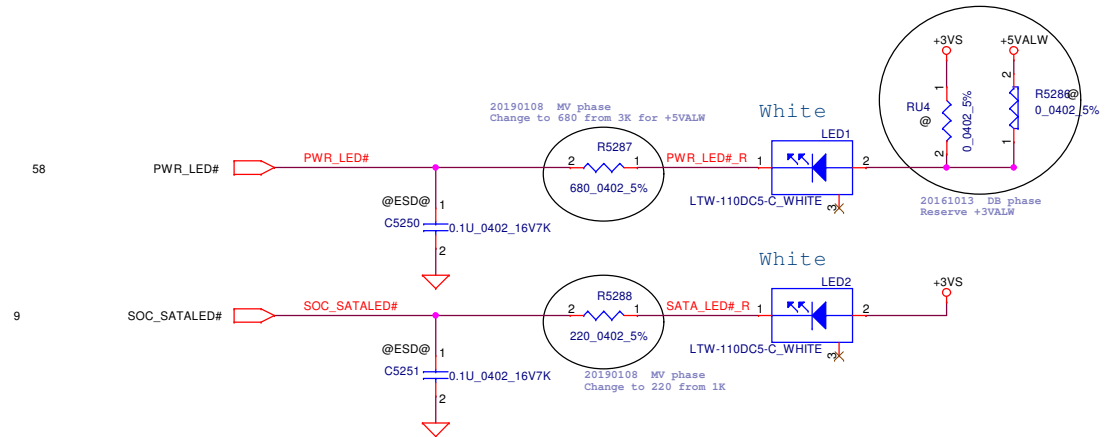
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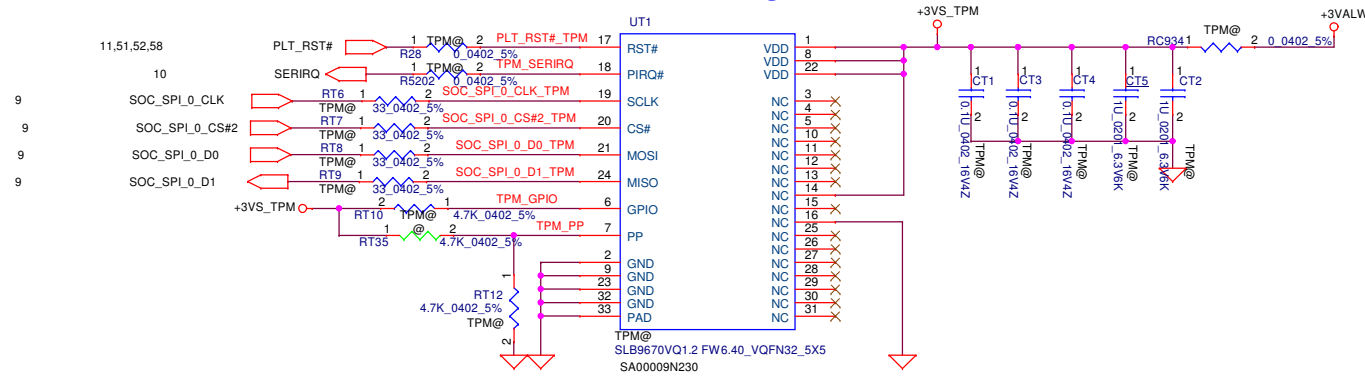
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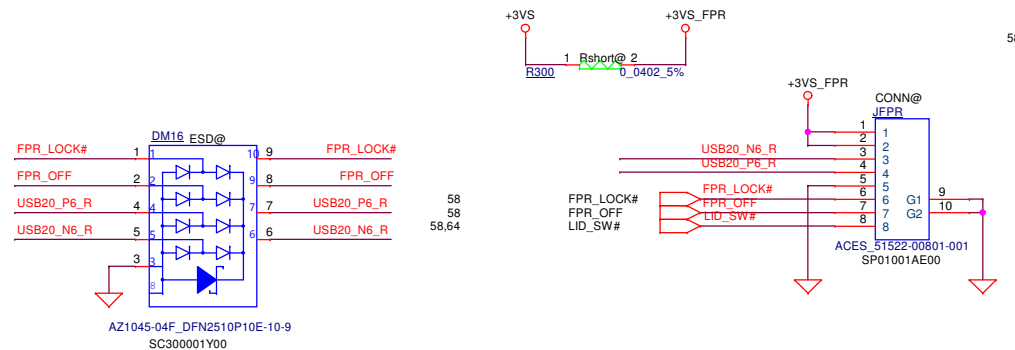
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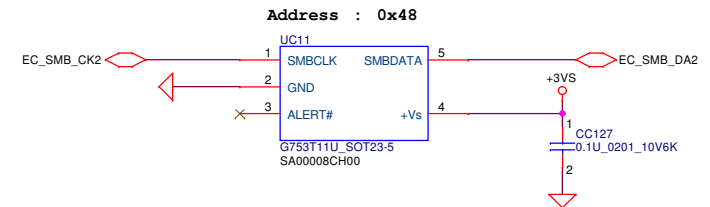
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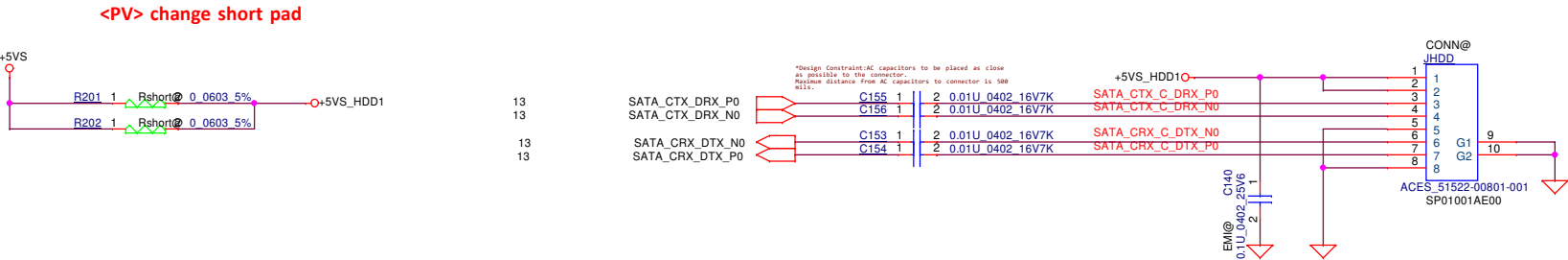


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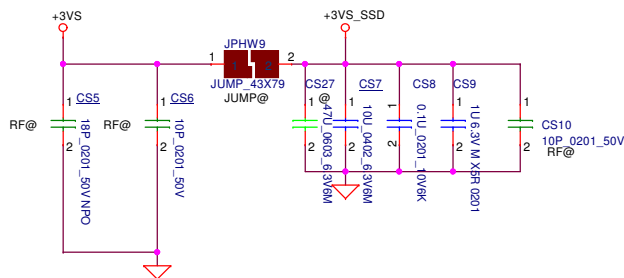


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2.5" SATA HDD



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Dwg No.		Sheet		67 of 100	



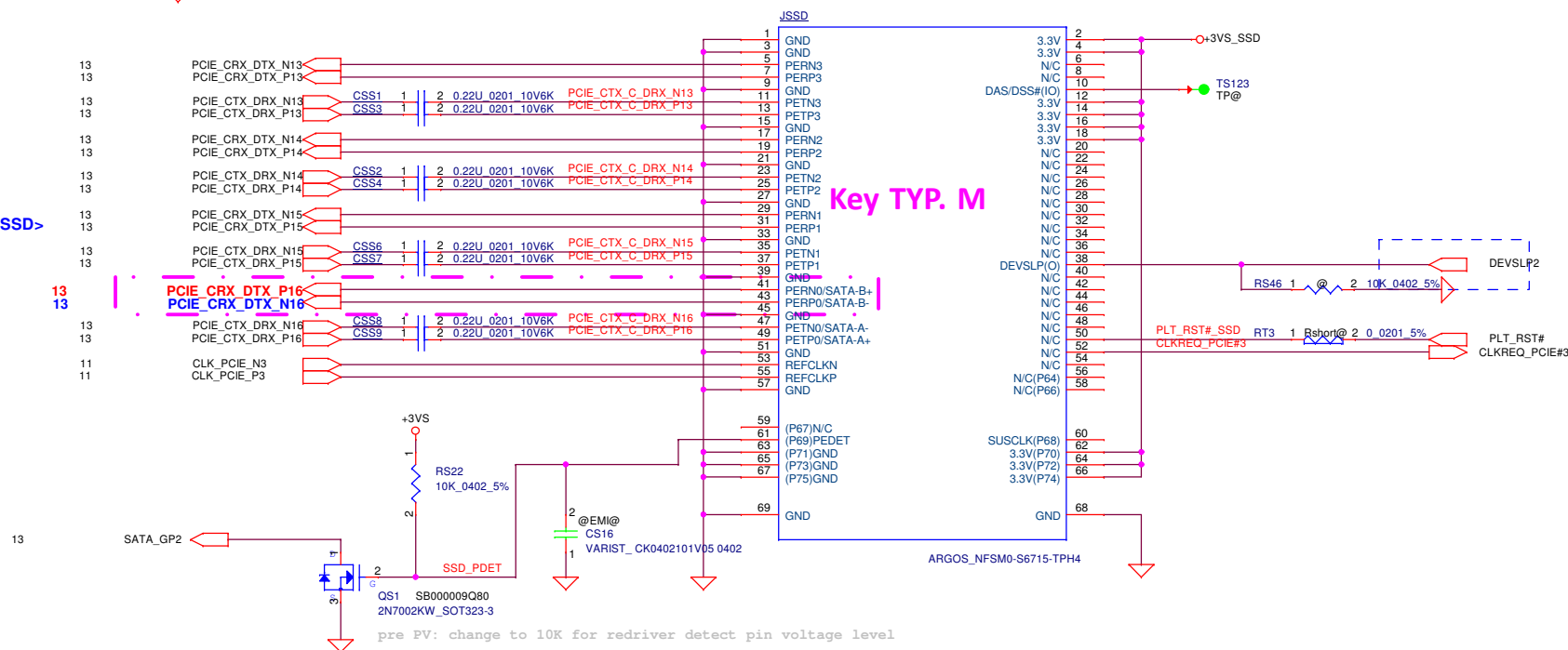
8,9,11,12,13,23,24,38,40,51,56,58,64,66,70,71,77,78,88

Figure 12-1. PCI Express® Link Configurations Supported by the Guidelines in this Chapter

PCIe Link Details	PCIe Controller #1	PCIe Controller #2	PCIe Controller #3
Line ID Lane #	1 2 3 4	5 6 7 8	9 10 11 12
PCIe Lane #	1 2 3 4	5 6 7 8	9 10 11 12
Base-U	AP 1 AP 2 AP 3 AP 4	AP 5 AP 6 AP 7 AP 8	AP 9 AP 10 AP 11 AP 12
Premium-U	AP 1 AP 2 AP 3 AP 4	AP 5 AP 6 AP 7 AP 8	AP 9 AP 10 AP 11 AP 12

<SSD>

Key TYP. M



36.3.2.4 AC Capacitor General Guidelines for M.2 SSD Storage Routing on SATA / PCI Express® Multiplexed Ports

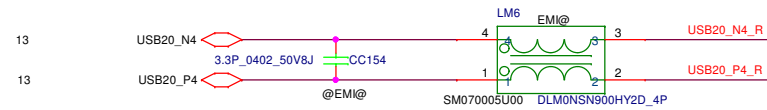
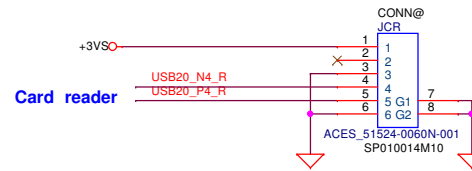
The following table summarizes the AC capacitor requirements on the motherboard when using the SATA/PCIe® multiplexed ports.

Note: When SATA and PCIe® are muxed, always route according to SATA design guidelines. SATA does not support signal polarity reversal and does not support lane reversal.

39	GND	PCleM/Mx_D09000NU90_MZVLW1T0HMH-000H1_F73H1Q_0FH	39	GND	Return Current Path	40	GND	Return Current Path
41	PETN0	PCle TX	42	N/C		43	TXN	Transmitter Differential Signal Pair
43	PETN1	PCle TX	44	N/C		45	TXN	Transmitter Differential Signal Pair
45	GND	Return current path	46	N/C		47	GND	Return Current Path
47	PERN0	PCle Rx	48	N/C		49	PERN1	Receiver Differential Signal Pair
49	PERN1	PCle Rx	50	PERST#		51	GND	Return Current Path
51	GND	Return current path	52	CLKREQ#				

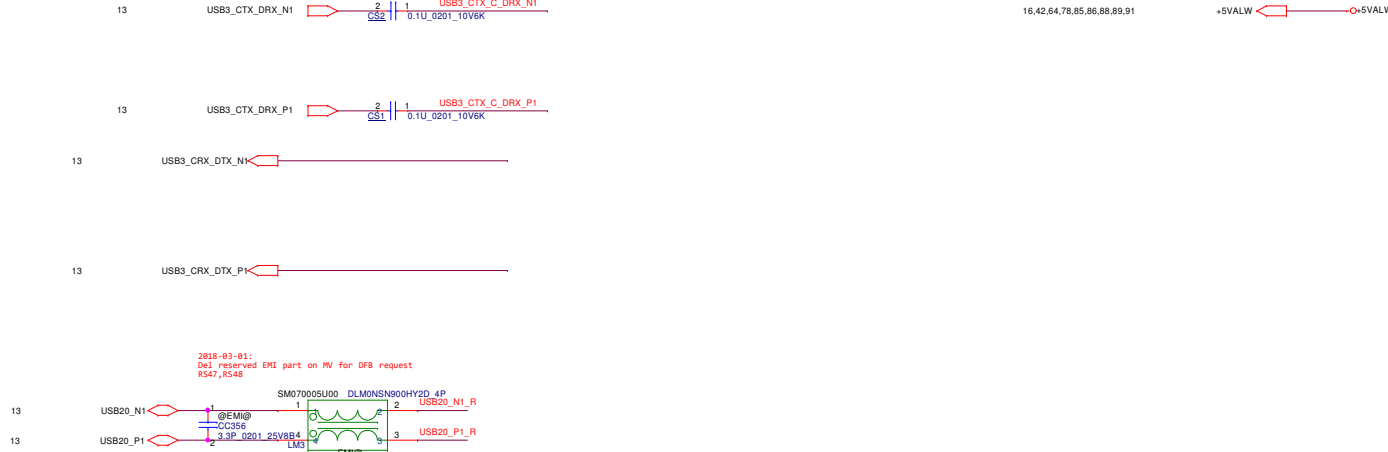
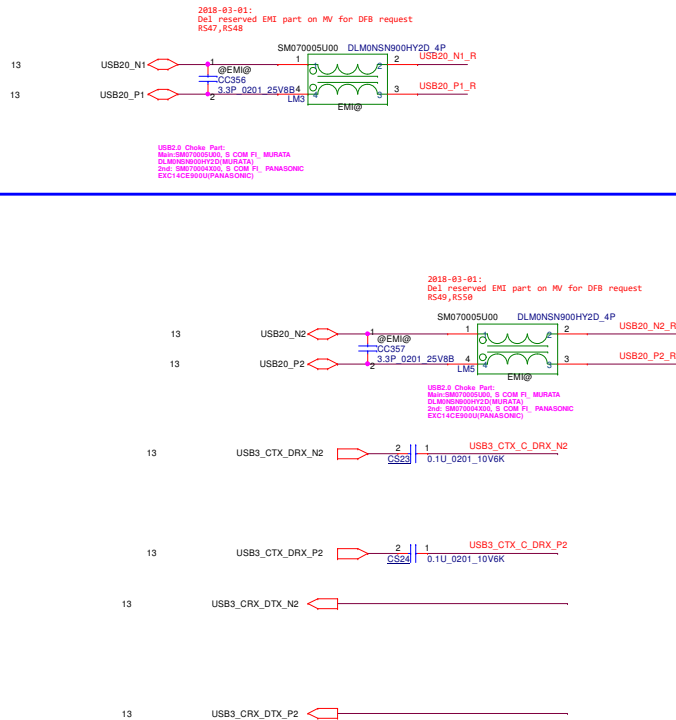
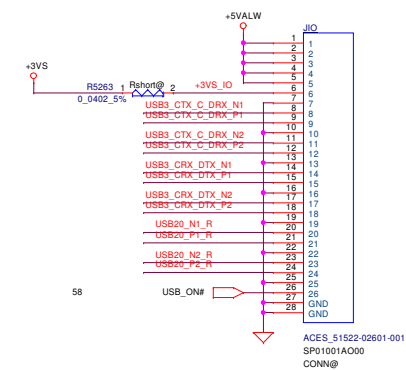
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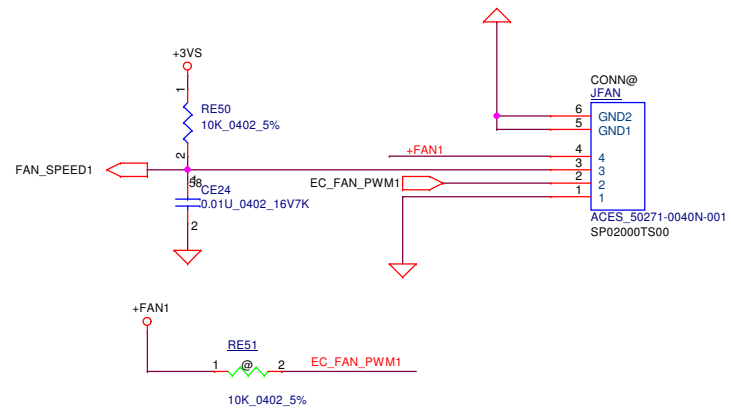
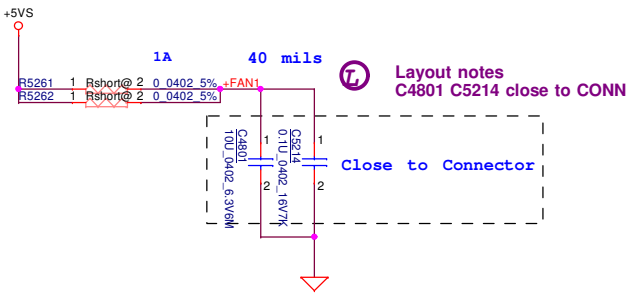
8,9,11,12,13,23,24,38,40,51,56,58,64,66,68,71,77,78,88 +3VS ← → +3VS



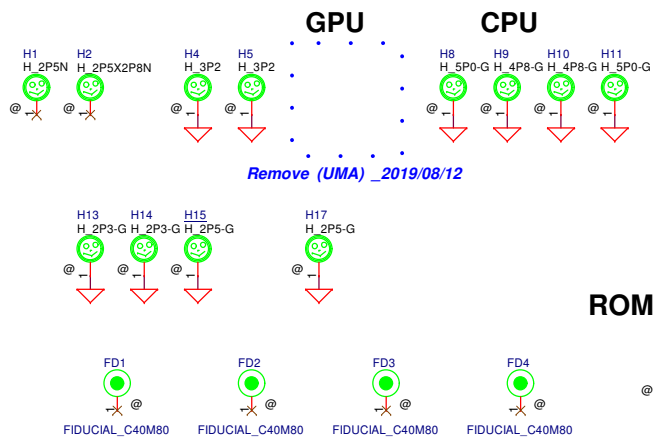
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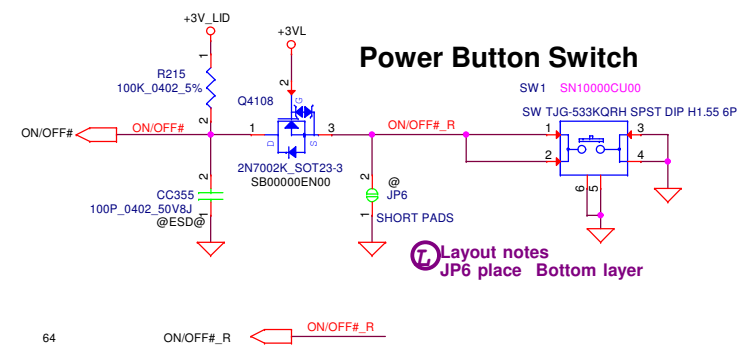




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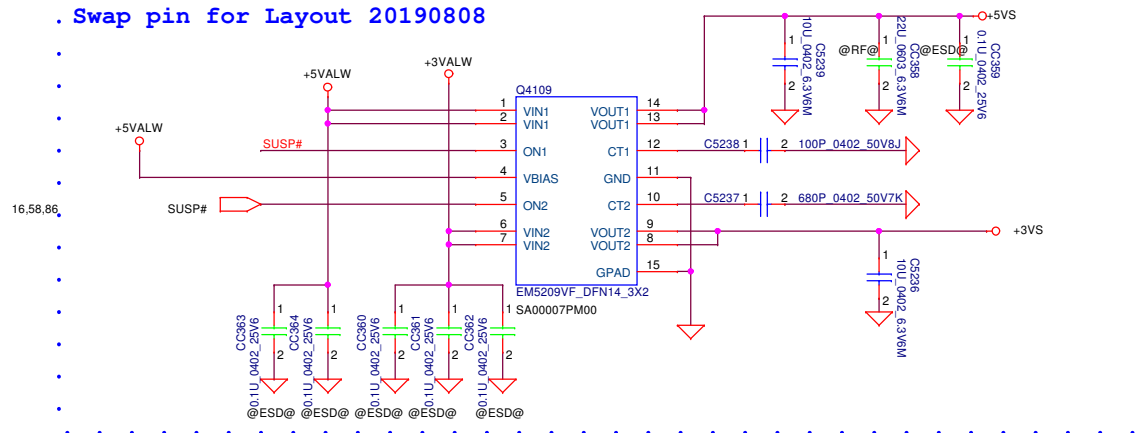


ROM STANOFF



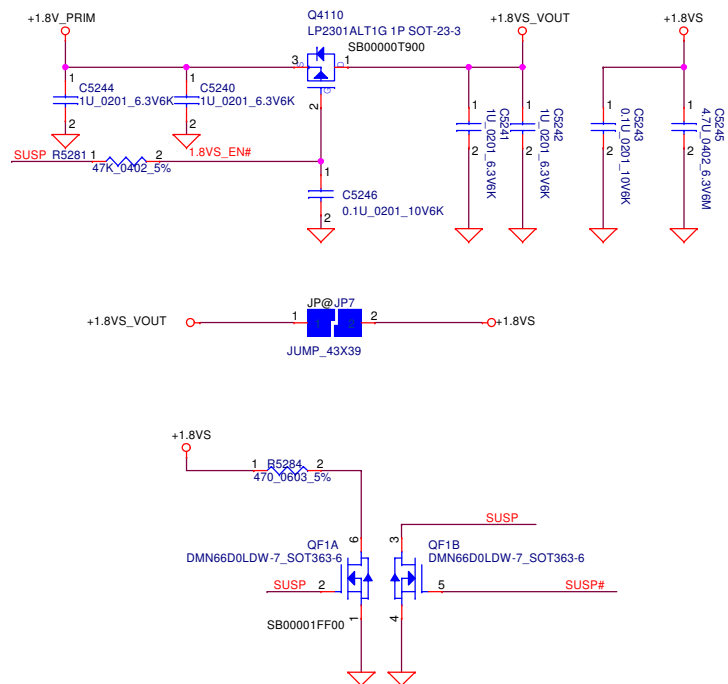
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Swap pin for Layout 20190808



+1.8V_PRIM TO +1.8VS

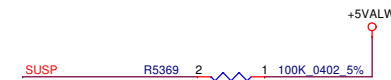
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RDS(max) : 150 mohm
V drop : 0.03V



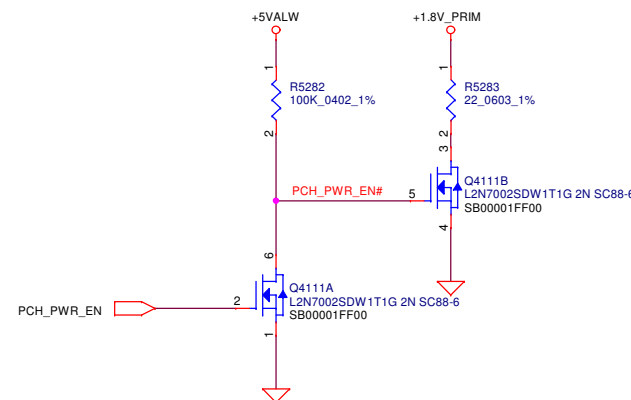
Add +1.8VS power down

+3VS
+5VS

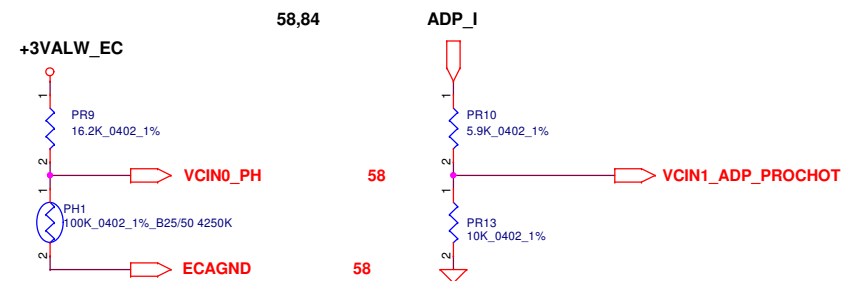
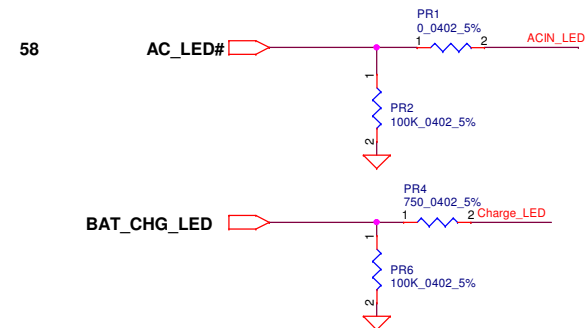
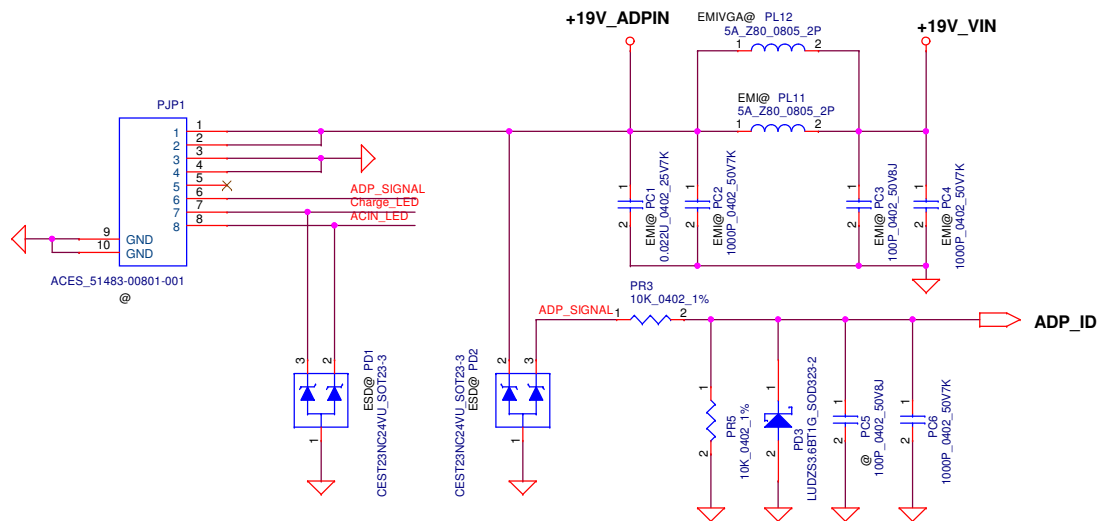
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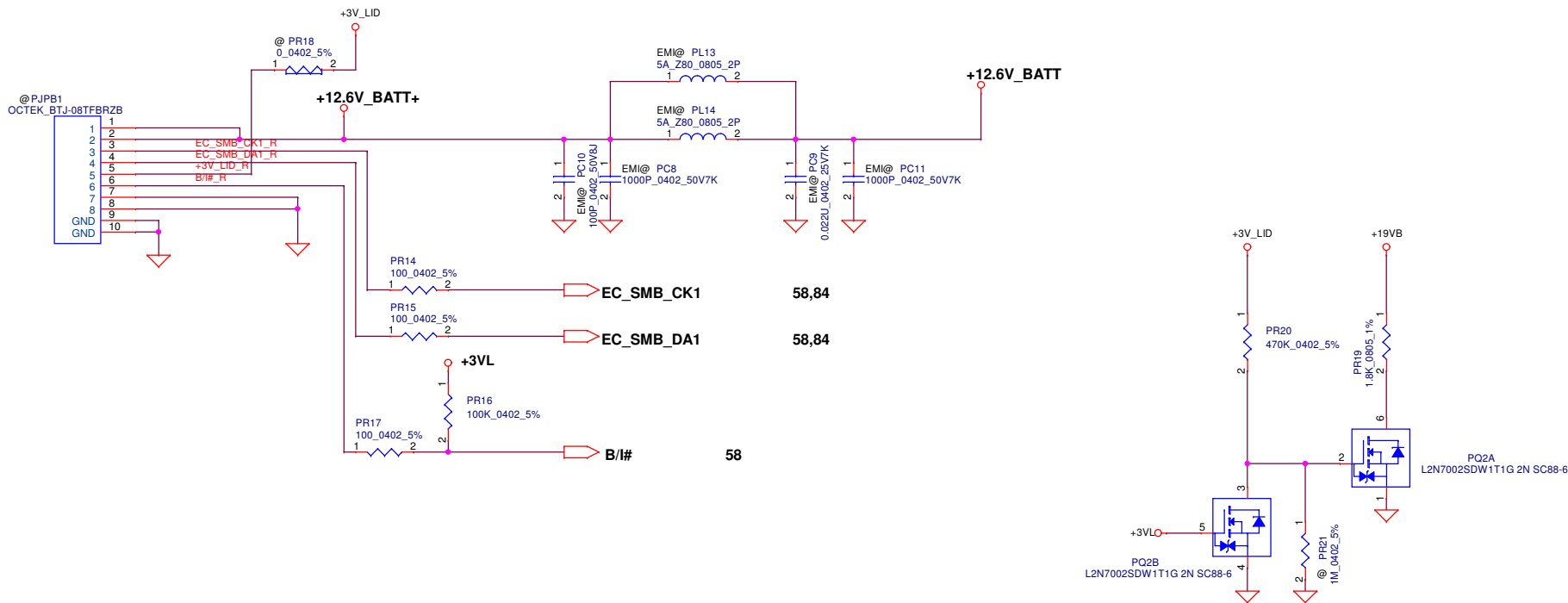
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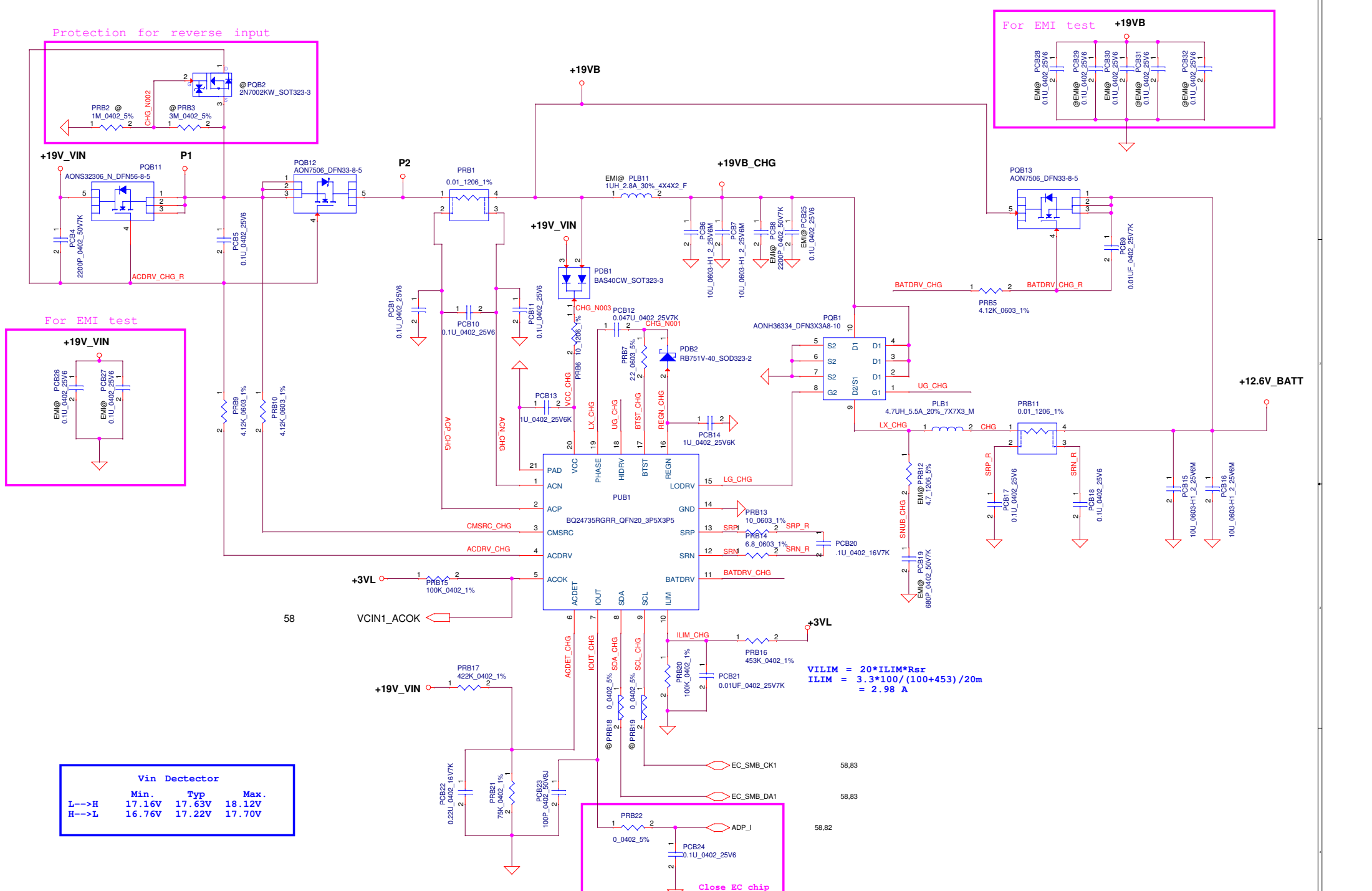
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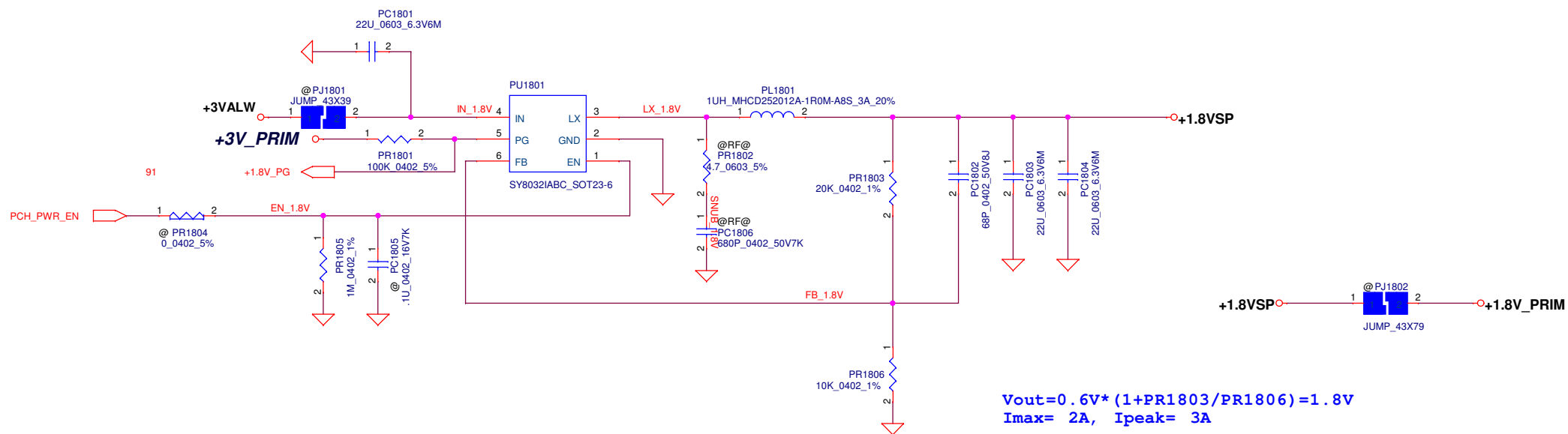
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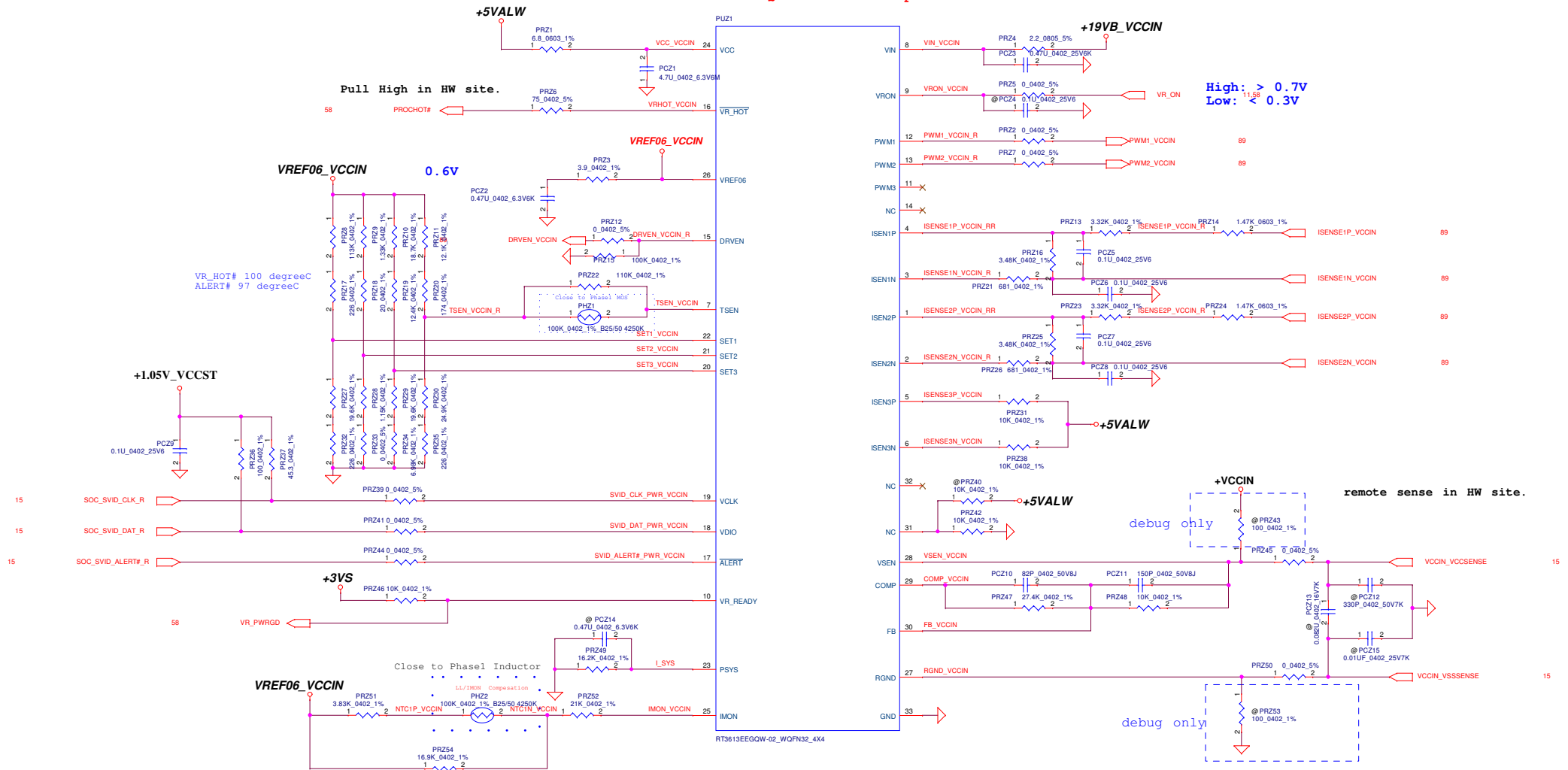


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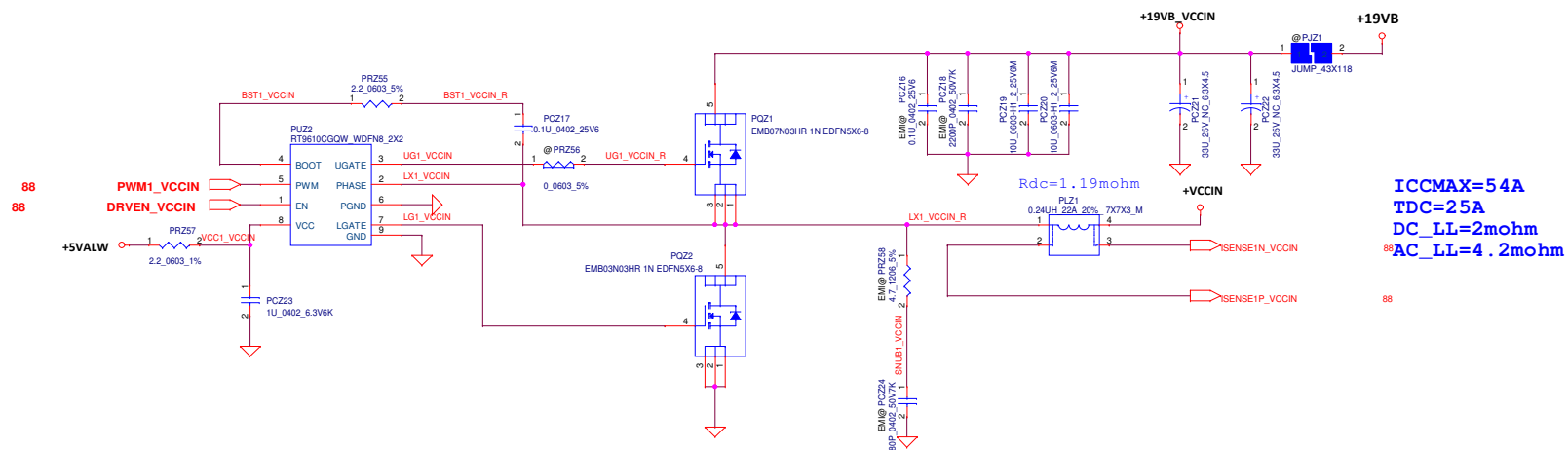
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RT3613EEGQW-02 is not MP part

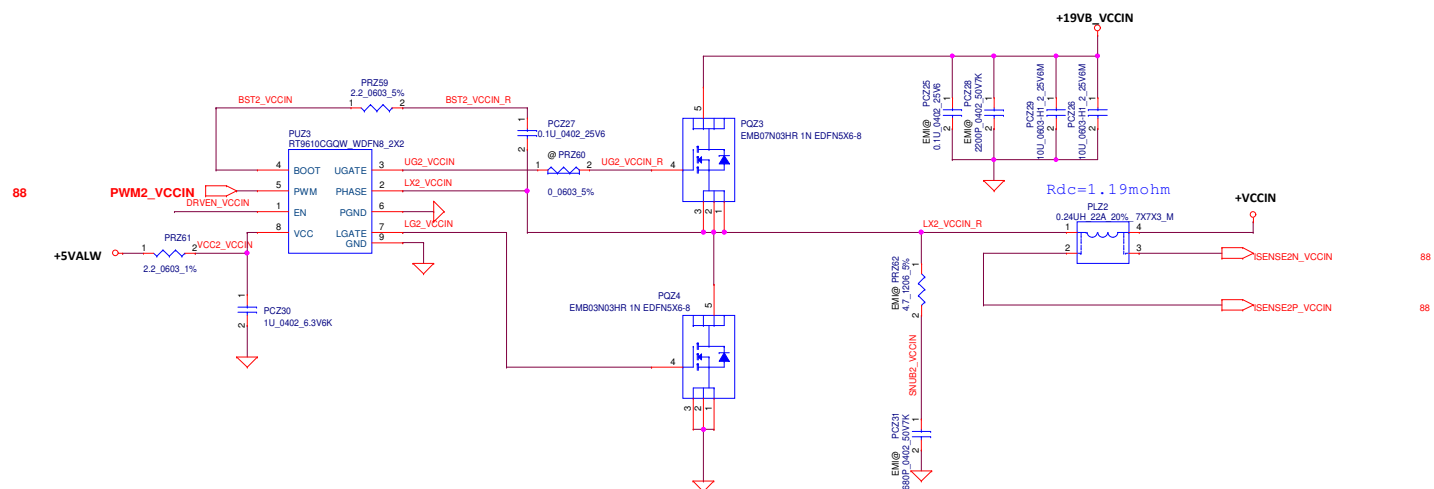


31 pin is a function to fix decay down slew rate to reduce acoustic noise.
High(5V): enable
Low(0V): disable
this pin can dynamic change state.

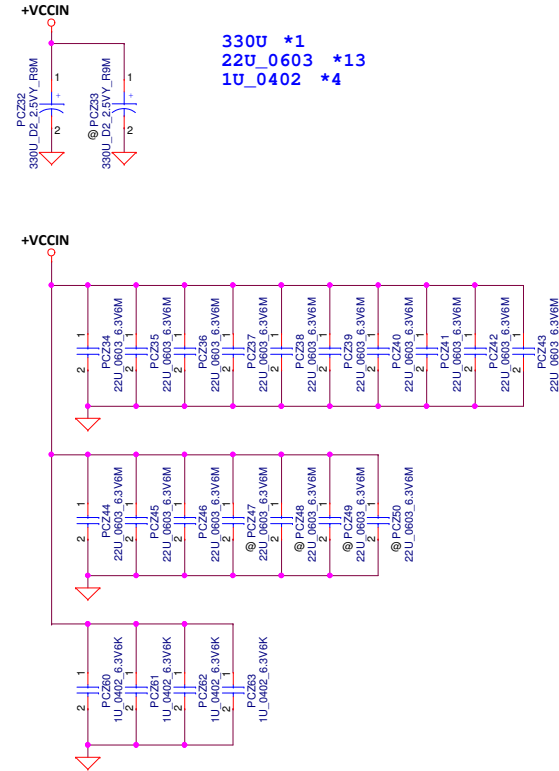
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TDC=25A
DC_LL=2mohm
AC_LL=4.2mohm
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